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A Novel Operation Method to Precisely Control Synaptic Strength for Phase-Change Artificial Synapse

You Yin*

Faculty of Science and Technology, Gunma University

1-5-1 Tenjin, Kiryu, Gunma 376-8515, Japan

*Corresponding author

<yinyou@gunma-u.ac.jp>

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Abstract. In this work, a novel operation method was proposed to control the synaptic strength in phase-change artificial synapse by applying staircase pulses. In the device, the recrystallization process was well controlled to achieve this aim. Simulation results exhibited that the phase change material was heated above its melting point during the first subpulse of the staircase pulse and then annealing temperature can be controlled by only varying amplitude of the second subpulse. This implied that the recrystallization region was precisely controllable by applying staircase pulses. Conductance (synaptic strength) change as a function of the amplitude of the second subpulse, which is caused by the growth and the shrinkage of recrystallized region, was obtained at each width of second subpulse.

1. Introduction

The demand for next generation devices with higher performance and better energy efficiency is rapidly increasing since transistor technology has moved closer and closer to the limits of Moore's law [1]. Researchers in the world have been trying to imitate the performance of the most efficient known computational entity, the human brain. It excels at very complicated tasks while it consumes very little energy as low as 20 W [2]. It presents an interesting computing model, made up of extremely dense networks of computing elements (neurons) with versatile memory elements (synapses). Scientists imitate neurons and synapse artificially using different materials based on different physical phenomena such as phase change and filament formation [3-8]. Many metal oxide synaptic devices based ionic diffusion and joule heating have been reported in recently years. For example, $Cu/NiO_y/NiO_x/Pt$ device showed a high on/off ratio of 10^3 but it had a short retention of 10^4 s [9]. $Pt/TiO_2/Pt$ showed an improved retention (5×10^4 s) but it has a very low on/off ratio of 2 [10]. The performance of this type of device depends strongly on both oxides and electrodes. Some sulfide synaptic devices based on atomic switch were also reported. These devices showed a very high on/off ratio ($>10^6$) but this technology has a bad CMOS compatibility [11]. The crystal phase alteration at high temperature >200 ℃ could affect the device performance [12]. Carbon nanotube (CNT) or graphene based synaptic devices showed a very high on/off ratio of 10^5 but there existed some difficulty in fabricating them [13]. It is difficult to locate CNT or grow graphene on substrates. The phase-change device attracts much attention due to its high performance such as low power, good reliability and ultrahigh speed [14-15]. However, there still exists some problem for this kind of synaptic devices from the point of view of the operation method. The transition from one state to other state is not easy to control. In this work, we proposed a novel method of application of staircase pulse to solve this problem. This method can be easier than the conventional one to precisely control the device conductance corresponding to the synaptic strength.

2. Principle of phase-change synaptic device

Figure 1 shows the principle of a phase-change synaptic device. Chalcogenides such as $Ge_2Sb_2Te_5$ are usually used as a media to store synaptic strength (weight) in phase-change synaptic device. As shown in Fig. 1(a), by applying a high and short electrical pulse to a phase change device, a programming volume of a chalcogenide alloy is heated to a temperature above the melting point (T_m) of the alloy and then the formerly melted part is quenched below a crystallization temperature (T_c) so rapidly that crystallization could be sufficiently prevented. The phase-change synaptic device then enters a lowly conductive amorphous state. This amorphizing operation is schematically shown as a red curve in Fig. 1(a). On the other hand, in the crystallizing operation as a dark blue dotted curve in Fig. 1(a), when a low and long electrical pulse is applied to heat the chalcogenide alloy to a temperature between T_m and T_c, the programmable volume of the chalcogenide alloy layer would crystallize, and, thus, a highly conductive crystalline state could be written into the synaptic device.

To collect analog information, it is fundamental to implement gradual conductance corresponding to synaptic strength to utilize synaptic plasticity with non-linearity and symmetry between long-term potentiation (LTP) and long-term depression (LTD), which generates neuronal activity through differences in the connection strength between the synapses. By applying different pulses and controlling the ratio of crystalline to amorphous phase, it is possible to obtain plasticity with LTP and LTD as shown in Fig. 1(b) in theory. However, it is difficult to realize such a gradual increase and decrease in conductance since the crystallization is so fast when an electrical pulse is applied. Besides this, the ratio of electrical conductivity of crystalline to amorphous could be as high as 5~7 orders of magnitude. This usually results an abrupt increase or decrease in conductance in practical devices.

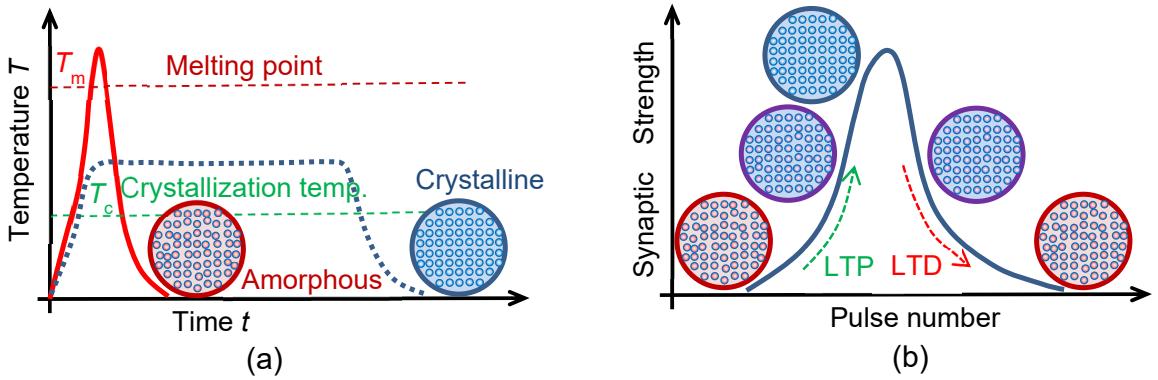

Fig. 1. (a) Schematic diagram of phase change process in phase-change synaptic. (b) Typical plasticity of a phase-change synaptic device showing long term potentiation (LTP) and long term depression (LTD).

3. Proposal of a novel operation method

The detailed approach to gradual conductance (synaptic strength) can be explained from programming methods as in Fig. 2. As is well known, a high and short electrical pulse as shown in Fig. 2(a) heats the phase change material above the melting point (T_m) and cool it down suddenly as shown in Fig. 2(d) to obtain the complete amorphous phase with the lowest crystallinity as shown in Fig. 2(g). On the other hand, an intermediate and long electrical pulse as shown in Fig. 2(b) heats the phase change material between the melting point and the crystallization temperature (T_c) and keeps the temperature during a certain period as shown in Fig. 2(e) to obtain the complete crystalline phase with the highest crystallinity as shown in Fig. 2(h). Here, we proposed a staircase-like shaped pulse as shown in Fig. 2(c) to firstly heat phase change material above T_m and then let it cool down and keep the temperature between T_m and T_c for a certain annealing period of t_c as shown in Fig. 2(f). The

staircase-like shaped pulse is composed of two sub-pulses for amorphization and subsequent control in crystallinity. The first amorphization sub-pulse with an amplitude of V_1 and a pulse width of t_1 is used for amorphizing the phase change material and the second crystallinity-control sub-pulse with an amplitude of V_2 and a pulse width of t_2 is used for controlling the total crystallinity from complete amorphous to complete crystalline phases as shown in Fig. 2(i). The two parameters of V_2 and t_2 of the second sub-pulse are of great importance for the control in the total crystallinity by the annealing temperature and time (t_c). Here, we mainly discuss the effect of the width t_2 of the second sub-pulse on the total crystallinity for gradual conductance (synaptic strength) here.

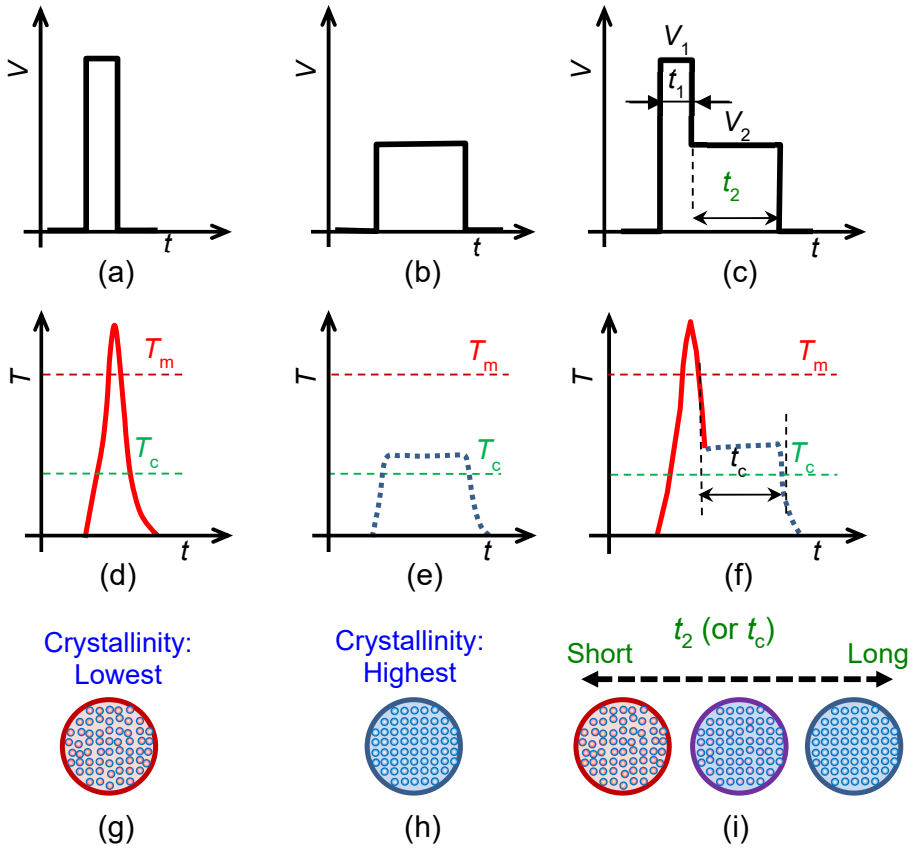

Fig. 2. Concept of control in total crystallinity for gradual conductance (synaptic strength). (a) High but short pulse. (b) Intermediate but long pulse. (c) Staircase-like shaped pulse. The high and short 1st sub-pulse with a time of t_1 and an amplitude of V_1 is used for amorphization of phase change material. The intermediate and long 2nd sub-pulse with a time of t_2 and an amplitude of V_2 is then used for control in total crystallinity after melting. (d) Schematic temperature profile caused by pulse shown in (a). (e) Schematic temperature profile caused by pulse shown in (b). (f) Schematic temperature profile caused by pulse shown in (c). (g) Amorphous phase with lowest crystallinity. (h) Completely crystalline phase with highest crystallinity. (i) Possible phases with different crystallinities, which could be obtained by varying the length of V_2.

4. Simulation results

The schematic structure used in simulation is shown in Fig. 3(a). Here, the synaptic device has a 150-nm-thick $Ge_2Sb_2Te_5$ (GST) layer as the active layer. We adopted most widely researched GST in this study. The defined GST part was connected by two underlying 50-nm-thick TiN electrodes. Figure

3(b) shows the highest temperature change in GST layer when staircase pulse is applied to two TiN electrodes. The simulation was conducted by using a commercially available finite-element analysis software COMSOL. In this study, we applied the first 50-ns and 8-V pulse and the second pulse with a certain width of 100 ns but variable heights from 0 to 6.4 V. The curve **a** shows the temperature profile induced by a simple pulse (t_2=0) of 8 V, 50 ns. The region between electrodes is heated above the melting point T_m. The quench time from its melting point to its crystallization temperature T_c is about 15 ns, which is short enough to keep the atoms in the highly disordered state and be amorphized. Then the annealing temperature can be controlled by applying a staircase pulse with a 8 V, 50 ns first subpulse and 100 ns second subpulse with an amplitude of 0-6.4 V. According to typical temperature distributions for pulses with second subpulse amplitudes of 3.2, 4.0, 4.8, and 5.6 V, it is obvious that the recrystallization region increases with second subpulse amplitude. This means that the recrystallization region can be controlled simply by the amplitude of the second subpulse. As is well known for the phase change materials, the higher the annealing temperature for a certain annealing time, the higher the crystallinity. The high crystallinity corresponds to a high conductance for a synaptic device. As a result, from our simulation, we can know that the synaptic strength can be well controlled by the applied staircase pulse.

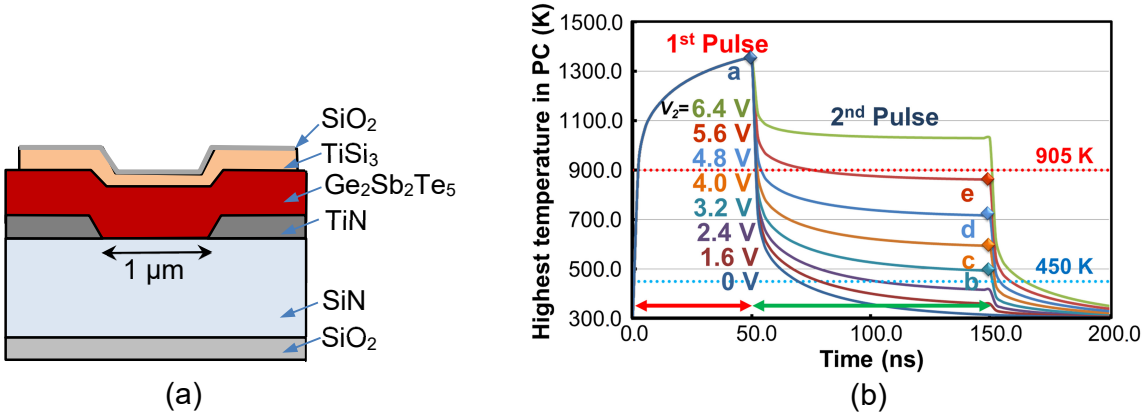

Fig. 3. (a) Structure used for finite element simulation. (b) Simulation results of highest temperature in phase-change (PC) layer.

5. Experimental results

In this study, we established the home made measurement system. It consisted of pulse application and resistance measurement controlled by LabVIEW, as shown in Fig. 4(a). A waveform generator (Model 2571, Tabor Electronics, Ltd.) was adopted to apply staircase pulses to the synaptic devices. Device resistance R was read out at a low voltage and device conductance (synaptic strength) was calculated after resistance reading.

The experimental results on the recrystallization control are shown in Fig. 4(b). The staircase pulses with a first subpulse of 8 V, 50 ns and a second subpulse of 0-5.6 V were applied to the device. The width of the second subpulse is 50, 100, 500 ns. The synaptic strength changed by more than one order of magnitude owing to the large recrystallization region when the wide 500 ns second subpulse was applied. This gradual change in conductance is very necessary for the synaptic device with LTP and LTD as described in the introduction part.

The device conductance changed a little at a small pulse amplitude V_2 of 1.4 V because the recrystallization started to occur between the two electrodes. The heating at a temperature between crystallization temperature and melting point took place in a small region and resulted in a partial recrystallization, accompanying a small conductance increase. The conductance further increased until

2.1 V when the recrystallization region became larger. The conductance almost did not change even after a pulse with a subpulse amplitude of 2.4 V. At this voltage range from 2.1 to 2.4 V, the heating temperature fell in the range between crystallization temperature and melting point. It is thus thought that the region between electrodes almost became fully crystallized. The device conductance decreased again from 2.6 V, which was caused by the decreased recrystallization region. The heating at a temperature higher than the melting point took place in the small region and resulted in a partial amorphization, accompanying a small conductance decrease. Finally, the device conductance returned to the low conductance level corresponding to the completely amorphous state.

This technology shown here is still at laboratory level and there is a long way to go for future's practical application. For example, high switching endurance should be obtained because the large number of computation times is required for the application of the brain-like computer. Some new phase-change materials and some new algorithms should be developed to solve this problem.

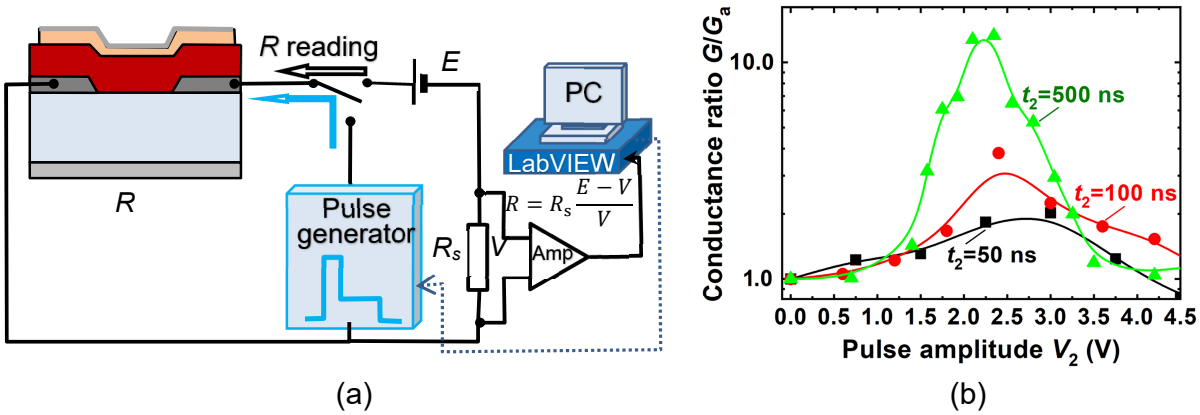

Fig. 4. (a) Circuits for the stairlike pulse application and measurement of synaptic devices. (b) Conductance (synaptic strength) change as a function of the amplitude of the second

6. Conclusions

The staircase pulse with two subpulses was proposed for programming the phase-change synaptic device for LTP and LTD. The second subpulse is critical to control the total crystallinity based on our simulation results. And experimental results showed that the synaptic strength (conductance) gradually increased and then decreased with increasing the amplitude of second subpulse during the enlargement and shrinkage of recrystallization region. This staircase pulse programming technique exhibited the possibility that synaptic strength can be well controlled.

Acknowledgements

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