# Short-Time INL Testing Methodology
# for High-Resolution ΔΣ ADC

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**Abstract.** This paper describes a mass production testing methodology for integral nonlinearity (INL) of a high precision ΔΣ analog-to-digital converter (ADC) in short time. We consider its INL testing by separating its analog and digital parts: ΔΣ AD modulator and digital filter. The digital filter can be tested with the scan-path method. For the AD modulator part, its nonlinear curve of the DC input-output characteristics can be obtained using a DC input varying with a fine step, but it takes an enormously long time; it is not practical for mass production testing. So we consider a polynomial model of the ΔΣ AD modulator input-output characteristics and estimate its coefficient values from the fundamental and harmonics power by applying a cosine input and obtaining the modulator 1-bit output power spectrum with FFT. Its INL can be estimated from the coefficients accurately when the modulator I/O characteristics is continuous. Our simulation and experimental results show that significant testing time reduction can be achieved with the proposed method.

## 1. Introduction

In recent years, Internet of Things (IoT) has attracted much attention, and the testing of IoT-related devices in short time with high quality has become more important at mass production shipping for the IoT system reliability [1-3]. This paper focuses on high-resolution low-sampling-rate ΔΣ ADCs, which are widely used with sensor interface circuits, such as air flow, temperature, pressure and strain gauge sensors as well as communication circuits [4-9]. However, its integral nonlinearity (INL) testing takes extraordinary long time; for example, let us consider the case of a 7 sample-per-second (sps) 24-bit ΔΣ ADC and 4 samples for each code used in its INL testing. Then its testing takes 111 days, which is not acceptable at all because the reasonable testing time is 1 second for 1 US dollar chip.

Therefore, in most cases, the INL testing for the ΔΣ ADC is omitted at mass production shipping. However, recently high quality and high reliable systems are demanded. Then we have developed its

INL testing algorithm with drastically reduced testing time as well as keeping good testing accuracy, and here we present its algorithm as well as simulation and experimental verifications.
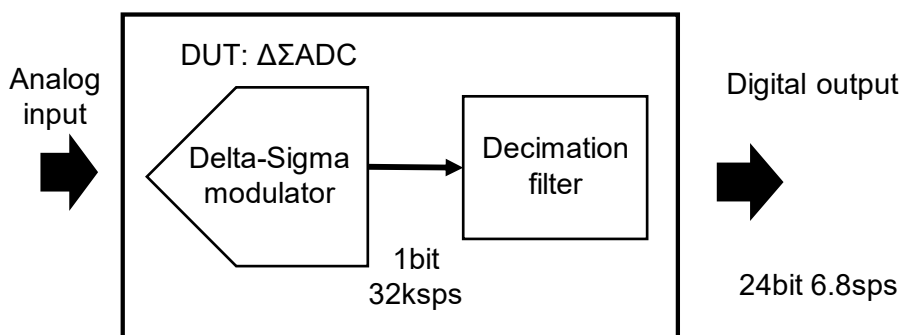


Fig.1. Configuration of a ΔΣ AD converter.

## 2. ΔΣADC

The ΔΣ AD converter is composed of a ΔΣ AD modulator in the analog section and a digital filter (decimator) in the subsequent stage [4-9]. The ΔΣ AD modulator performs ΔΣ modulation for the analog input with oversampling, so that noise shaping for the quantization noise is realized. Then 1-bit digital data stream is provided as the modulator output, which is fed to the following digital filter for low-pass filtering and decimation; its output is the entire ADC digital output (Fig. 1).

## 3. Proposed ΔΣ ADC Linearity Test Method

We consider a 7-sps 24-bit discrete-time ΔΣADC for the target application. Notice that only 7 digital output data can be obtained in 1 second, and hence the direct INL testing is not acceptable at all (Fig. 2). Hence, we consider here to observe the 32-sps 1-bit data stream of the ΔΣAD modulator for the INL testing. Notice also that the INL of the overall ΔΣADC is determined only by the ΔΣAD modulator, and the digital filter does not affect the overall ADC INL if it is well-designed and functional (i.e., without any catastrophic faults). Then we propose the following INL testing method (Fig. 3):

(1) Separate the AD modulator and the digital filter parts, and test them individually.

(2) The digital filter part is tested by the scan path method whether there are fatal faults. Notice that the digital filter part does not cause the overall ΔΣAD linearity deterioration unless it is faulty.

(3) The 1-bit output data stream of the ΔΣAD modulator is externally outputted through a test pin in test mode (Fig. 3), and it is observed during the test. Its output rate is 32ksps, which is much faster than the digital filter (decimator) output rate (7sps).

(4) Since the ΔΣ AD modulator contains an analog circuit, then even if there is not a fatal fault, its linearity may be degraded by parametric faults such as parasitic circuit components, which should be checked by the testing. It is assumed here that the input /output characteristics of the ΔΣ AD modulator do not have jumps (discontinuities), which is different from pipelined ADCs and SAR ADCs (Fig. 4).

(5) We model the input/output characteristics of the ΔΣ AD modulator including nonlinearity characteristics model with polynomials.

Let $x(t)$ be an input of the modulator and $y(t)$ be its output data stream, and then we model its input/output characteristics with the following n-th order polynomial model:

$$y(t) = a_0 + a_1 x(t) + a_2 x(t)^2 + \cdots + a_n x(t)^n \tag{1}$$

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(6) We apply a cosine wave to the modulator as follows:

$$x(t) = A\cos(\omega t) \tag{2}$$

Here, the amplitude of $A$ is known, and the input signal frequency $\omega$ as well as the sampling clock frequency $\omega s$ are low so that the modulator does not show high-frequency performance degradation. Then substituting Eq. (2) into Eq. (5), the modulator 1-bit output data stream is modeled by

$$y(t) = b_0 + b_1\cos(\omega t) + b_2\cos(2\omega t) + \cdots + b_n\cos(n\omega t) \tag{3}$$

Using the coefficients $a_0, a_1, a_2, \cdots, a_n$, the coefficients $b_0, b_1, b_2, \cdots, b_n$ can be expressed as follows [10, 11]:

$$\left.\begin{aligned}
b_0 &= a_0 + \frac{1}{2}a_2 A^2 + \frac{3}{2^3}a_4 A^4 + \cdots \\
b_1 &= a_1 A + \frac{3}{2^2}a_3 A^3 + \frac{5}{2^3}a_5 A^5 + \cdots \\
b_2 &= \frac{1}{2}a_2 A^2 + \frac{1}{2}a_4 A^4 + \frac{15}{2^5}a_6 A^6 + \cdots \\
b_3 &= \frac{1}{2^2}a_3 A^3 + \frac{5}{2^4}a_5 A^5 + \frac{21}{2^6}a_7 A^7 + \cdots \\
b_4 &= \frac{1}{2^3}a_4 A^4 + \frac{1}{2^4}a_6 A^6 + \frac{7}{2^5}a_8 A^8 + \cdots \\
b_5 &= \frac{1}{2^4}a_5 A^5 + \frac{7}{2^6}a_7 A^7 + \frac{9}{2^6}a_9 A^9 + \cdots \\
&\quad\vdots \\
b_{n-1} &= \frac{a_{n-1}}{2^{n-2}} A^{n-1} \\
b_n &= \frac{a_n}{2^{n-1}} A^n
\end{aligned}\right\} \tag{4}$$

(7) We perform FFT to the 1-bit output data stream of the modulator and obtain $b_0, b_1, b_2, \cdots, b_n$; then we derive $a_0, a_1, a_2, \cdots, a_n$ from the relation in Eq. (4). Now we have the following DC input/output characteristics:

$$y(t) = a_0 + a_1 + a_2 x^2 + \cdots + a_n x^{\,n} \tag{5}$$

(8) Finally we calculate the INL of the modulator from Eq. (5) using the end-point method or the best-straight-line method [1].

**Remark:** In this paper, we use the end-point method for obtain INL.

**Example:** Consider the case that the 3rd-order nonlinearity is the dominant distortion for the modulator. Then we model its input/output characteristics as follows:

$$y(t) = a_1 x(t) + a_3 x(t)^{\,3} \tag{6}$$

Provide to the modulator a cosine wave input $x(t)$ whose amplitude $A$ is known.

$$x(t) = A\cos(\omega t)$$

Then the modulator output $y(t)$ modeled in Eq. (6) is given as follows:

$$y(t) = a_1 x(t) + a_3 x(t)^{\,3} = \left(a_1 \cdot A + \frac{3}{4}a_3 \cdot A^3\right)\cos(\omega t) + \frac{1}{4}a_3 \cdot A^3 \cos(3\omega t) \tag{7}$$

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We perform FFT to y(t) and obtain its power spectrum. Then its fundamental spectrum power is given as follows:

$$b_1 = a_1 \cdot A + \frac{3}{4} a_3 \cdot A^3 \tag{8}$$

Its third harmonic spectrum power is expressed as follows:

$$b_3 = \frac{1}{4} a_3 \cdot A^3 \tag{9}$$

We can estimate the polynomial coefficients $a_1$, $a_3$ in Eq. (6) from $b_1$, $b_3$, and $A$, using the relationship among $a_1$, $a_3$, $b_1$, $b_3$, and $A$ in Eqs. (8), (9). Now we can estimate the AD $\Delta\Sigma$ modulator characteristics given by Eq. (6) and then calculate the overall ADC INL with the end-point method.
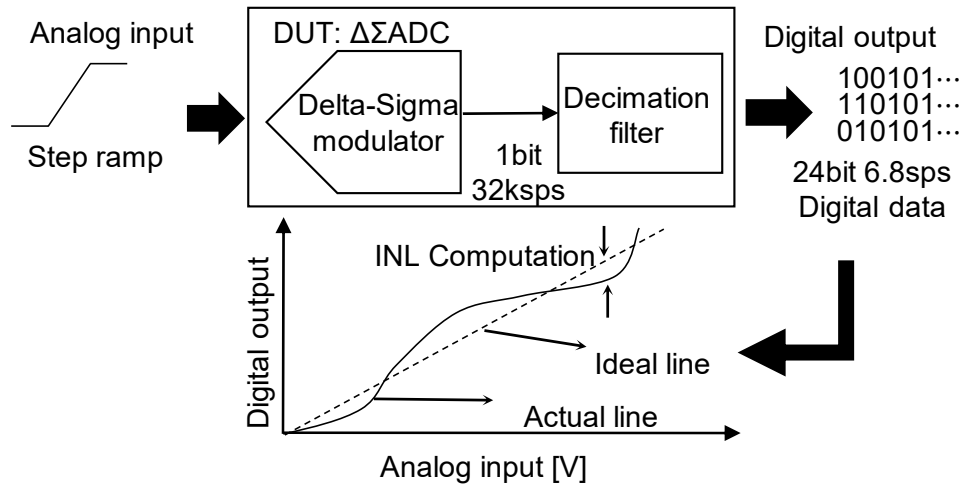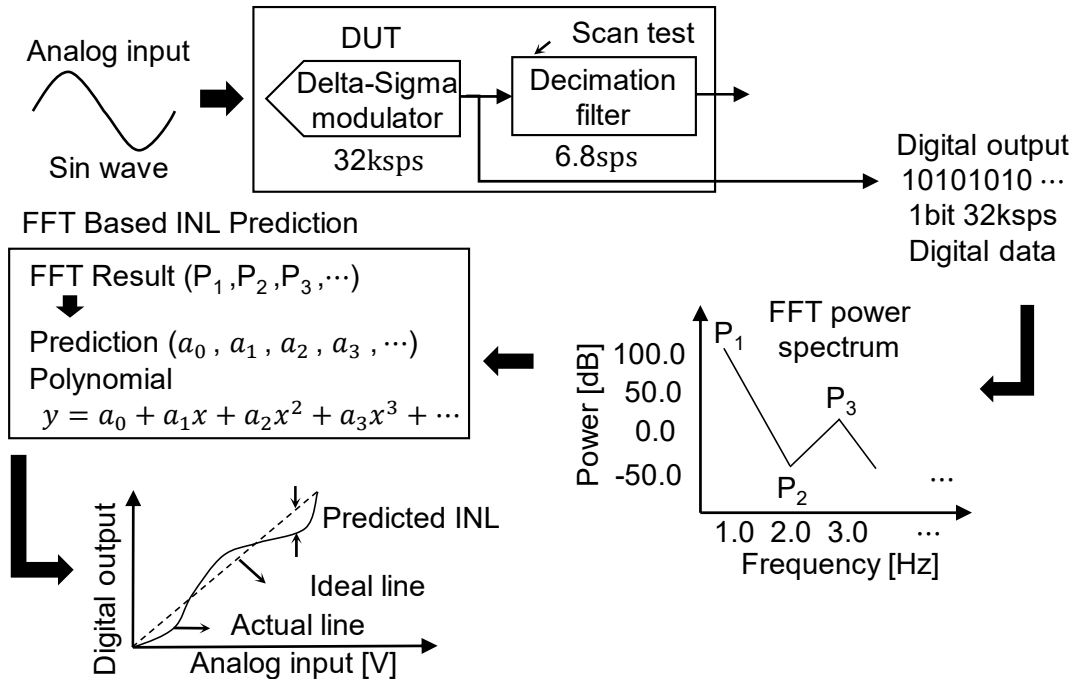


Fig. 2. All code testing for INL testing.
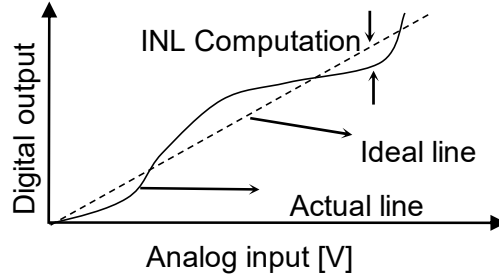


Fig.3. Proposed FFT-based INL prediction method.

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Fig. 4. Input/output characteristics of the ΔΣAD modulator without jumps.

## 4. Simulation Verification of Proposed Integral Linearity Test for ΔΣ AD modulator

### 4.1 Simulation Conditions

Section 4 shows simulation verifications of the proposed method in Section 3, in the following cases:
(i) Discrete-time 1st-order and 2nd-order modulators.
(ii) 3rd-order and 5th-oder nonlinearities.
(iii) Several nonlinearity strength variations.
(iv) Several input cosine wave amplitudes.
(v) Several cases for the number of acquired 1-bit data stream of the modulator output.
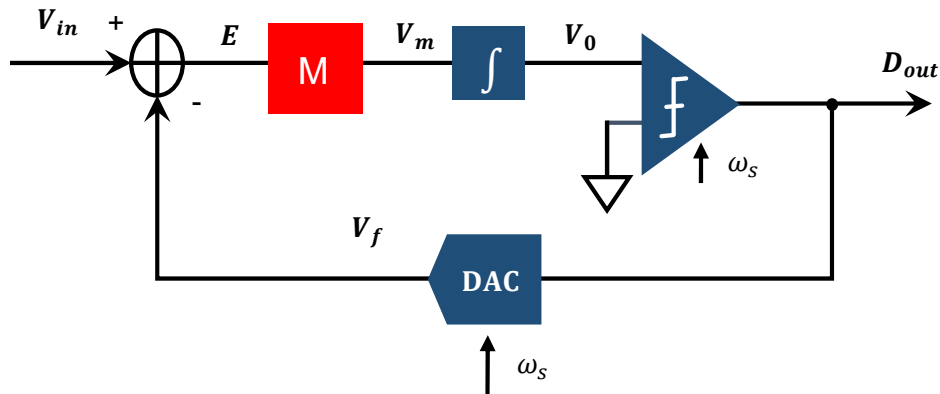Fig. 5 shows our simulation model of the 1st-order ΔΣ AD modulator with nonlinearities.



Fig.5. Simulation model of the $1^{st}$ - order ΔΣAD modulator with nonlinearity.

Here

$$E(n) = V_{in}(n) - V_f(n)$$
$$V_o(n) = V_o(n-1) + V_m(n)$$
$$\text{If} \quad V_o(n) \geq 0, \text{then}$$
$$D_{out}(n+1) = 1; \ V_f(n+1) = 1$$
$$\text{Else} \ D_{out}(n+1) = 0; \ V_f(n+1) = -1$$

The block M models the modulator nonlinearity and its nonlinearity strength can be controlled by the parameter $k$. Also notice that the block diagram in Fig. 5 is for system level simulation with MATLAB; in the actual circuit, the DAC output ($V_f$) is $V_{ref}$ for $D_{out} = 1$, or $-V_{ref}$ for $D_{out} = 0$, and the range of the ADC input ($V_{in}$) is from $-V_{ref}$ to $V_{ref}$.
In case that $3^{rd}$-order nonlinearity is dominant, we use

$$V_m(n) = E(n) - k * E(n)^3 \quad (k > 0) \tag{10}$$

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In case that $5^{th}$-order nonlinearity is dominant, we use

$$V_m(n) = E(n) - k * E(n)^5 \quad (k > 0) \tag{11}$$

In subsections 4.2 - 4.6, we consider the $3^{rd}$ - order harmonics is dominant and use Eq. (10), whereas in subsection 4.6 we consider also $5^{th}$-order harmonics is dominant and use Eq. (11).

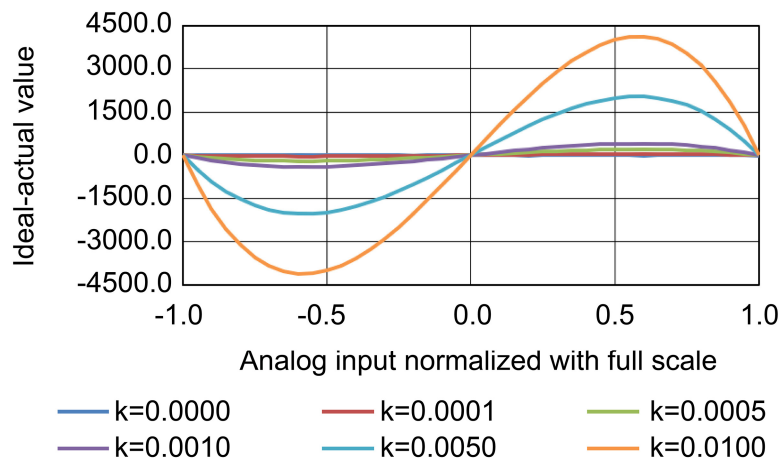### 4. 2 DC Input-Output Characteristics with Curve Fitting

In our first simulation, we apply a DC input to the $1^{st}$-order modulator input $V$in in Fig. 5, from -1 to 1 with 0.05 step and obtain its input/output characteristics as a reference, even though it takes quite a large number of AD modulator samplings. The number of 1's ($D_{out}$ = 1) for each DC value is obtained using $2^{20}$ data for a given DC input: the input DC value is changed with 0.05 step so that the total sampling number to obtain the whole input/output is enormous. The value of $k$ representing the strength of the nonlinearity is varied as 0.0000, 0.0001, 0.0005, 0.0010, 0.0050, 0.0100, and the number of 1's at $D_{out}$ is plotted in Fig. 6, which is the DC input/output characteristics and the INL of the modulator in Fig. 5.

The input/output characteristics in Fig. 5 are polynomial approximated by the following formula:

$$y = a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 \tag{12}$$
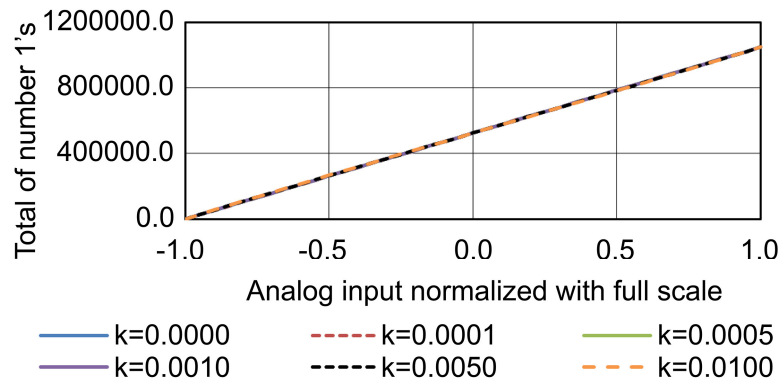


(a) Modulator output number of 1's



(b) Difference between the ideal and actual modulator output numbers of 1's.

Fig. 6. Simulation results of the DC input/output characteristics and the INL of the ΔΣAD modulator in Fig. 5 when the number of the modulator output is $2^{20}$.

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Table 1 shows the values $a_1$, $a_3$ obtained from the simulation results in Fig. 6 using the curve fitting for each $k$, $a_0$, and $a_2$, are relatively very small due to the nonlinearity model usage of Eq. (10). So they can be ignored and are not written in Table 1. We see the followings from Table 1:
  (1) As the value of $k$ increases, the value of $a_1$ slightly decreases.
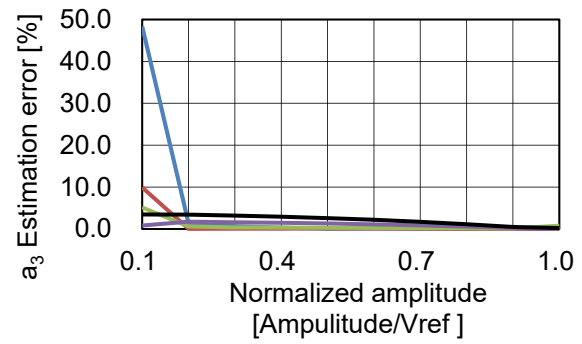  (2) As the value of $k$ increases, the value of $a_3$ increases.

Table.1 Estimated coefficient values in the polynomial model of the ΔΣ modulator DC input/input characteristics.

| $k$ | $a_1$ | $a_3$ |
|---|---|---|
| 0.0001 | 524180 | 104.84 |
| 0.0005 | 523760 | 524.48 |
| 0.0010 | 523240 | 1050.50 |
| 0.0050 | 519000 | 5282.50 |
| 0.0100 | 513610 | 10643.00 |
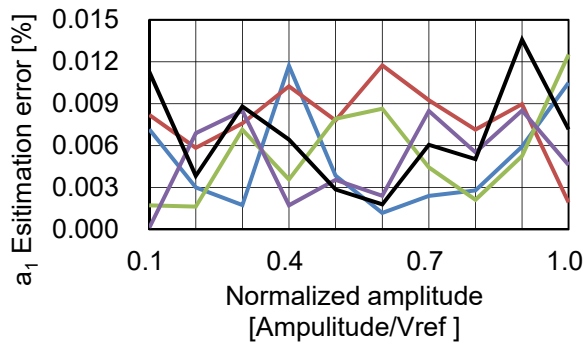
(a) $a_1$ estimation error (input: 0.1 ~ 1.0)
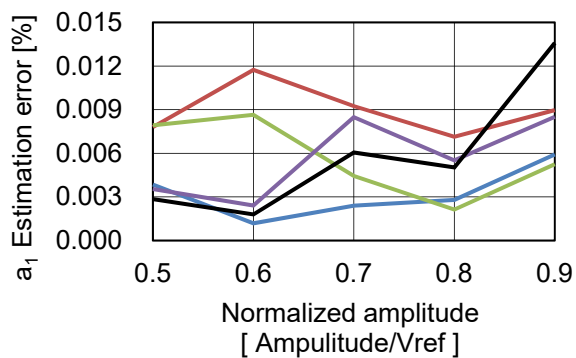
(b) $a_3$ estimation error (input: 0.1 ~ 1.0)
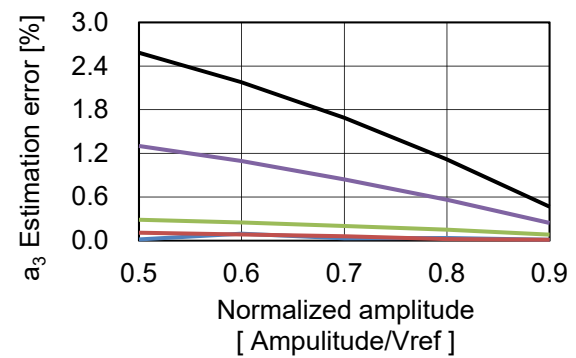
(c) $a_1$ estimation error (input: 0.5 ~ 0.9)

(d) $a_3$ estimation error (Input: 0.5 ~ 0.9)

Fig. 7. Estimation errors of the polynomial coefficients obtained from the 1st-order modulator output power spectrum.

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### 4.3 Cosine Wave Input and Output Power Spectrum

Next, we consider to provide a cosine wave to the AD modulator as $V$in (Eq. (2), Fig. 3), and obtain its 1-bit output stream of $2^{20}$ data. Then we perform FFT for the 1-bit output data stream and obtain its power spectrum; the fundamental wave power $P_1$ and the third harmonic power $P_3$ (Fig. 7). Here $\omega_{in}/\omega_s = 1/2^{20}$, $\omega_{in}$ is an input angular frequency and $\omega_s$ is a sampling angular frequency.

As the number of the acquired modulator output data is large, the estimation accuracy for $a_1$, $a_3$ improves; we found that $2^{20}$ is a reasonable compromise between testing time and accuracy for both the 1st-order and 2nd-order modulators.

### 4.4 Estimation of Polynomial Coefficients with Proposed Method

Polynomial modeling is performed for the DC input/output characteristics of the $\Delta\Sigma$ AD modulator, based on Eq. (6). Then we estimate the values of $a_1, a_3$ from $P_1$ and $P_3$ obtained in Fig. 8, using Eqs. (8) and (9). Fig. 7 shows the errors of $a_1, a_3$ between these estimates and the ones in Table 1.
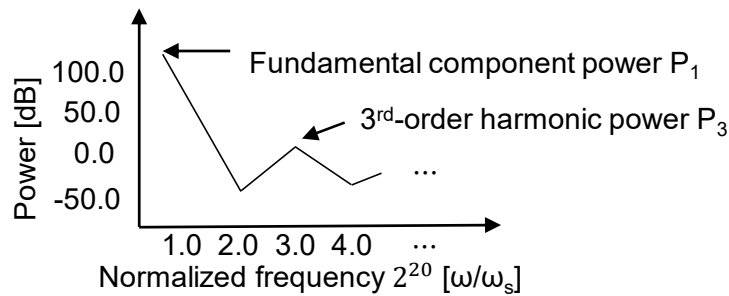


Fig. 8. Simulation result of the $\Delta\Sigma$ modulator output power spectrum obtained by FFT for a cosine wave input.

### 4.5 2nd-order Modulator Case

A 2nd-order modulator in Fig. 9 with $2^{20}$ samples is also simulated with the same method. Fig. 10 shows the estimation errors of the fundamental and 3rd harmonics for the input with the amplitude of 0.5 to 0.9 from the 2nd-order modulator output power spectrum. We see the following from Fig. 8 and Fig. 10:

(1) Estimation error for $a_1$ is small for all the input amplitude $A$.

(2) When the input amplitude $A$ increases to 0.9, then the estimation error for $a_3$ is reduced. Notice that the input amplitude $A$ is controllable during testing time.

(3) Notice that if the number of data is reduced compared to $2^{20}$, the estimation error becomes larger than the one as shown in Fig. 6 and Fig. 7.

(4) By comparing the 1st-order modulator with the 2nd-order modulator, the estimation errors of the both models are small. So we expect that this method is applicable for testing also high-order modulators.
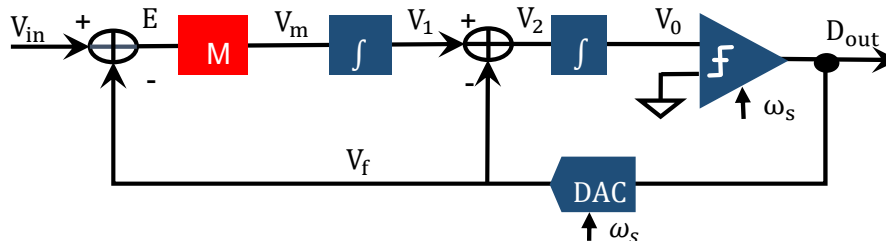


Fig. 9. Simulation model of the 2nd -order $\Delta\Sigma$AD modulator with nonlinearity.

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Here

$$E(n) = V_{in}(n) - V_f(n)$$
$$V_1(n) = V_1(n-1) + V_m(n)$$
$$V_2(n) = V_1(n) - V_f(n)$$
$$V_o(n) = V_o(n-1) + V_2(n)$$
$$\text{If} \quad V_o(n) \geq 0, \text{then}$$
$$D_{out}(n+1) = 1; \; V_f(n+1) = 1$$
$$\text{Else} \; D_{out}(n+1) = 0; \; V_f(n+1) = -1.$$

The block M models the modulator nonlinearity and its nonlinearity strength can be controlled by the parameter $k$. In case that 3rd-order or 5th - order nonlinearity is dominant, we use Eq. (10) or Eq. (11) respectively.
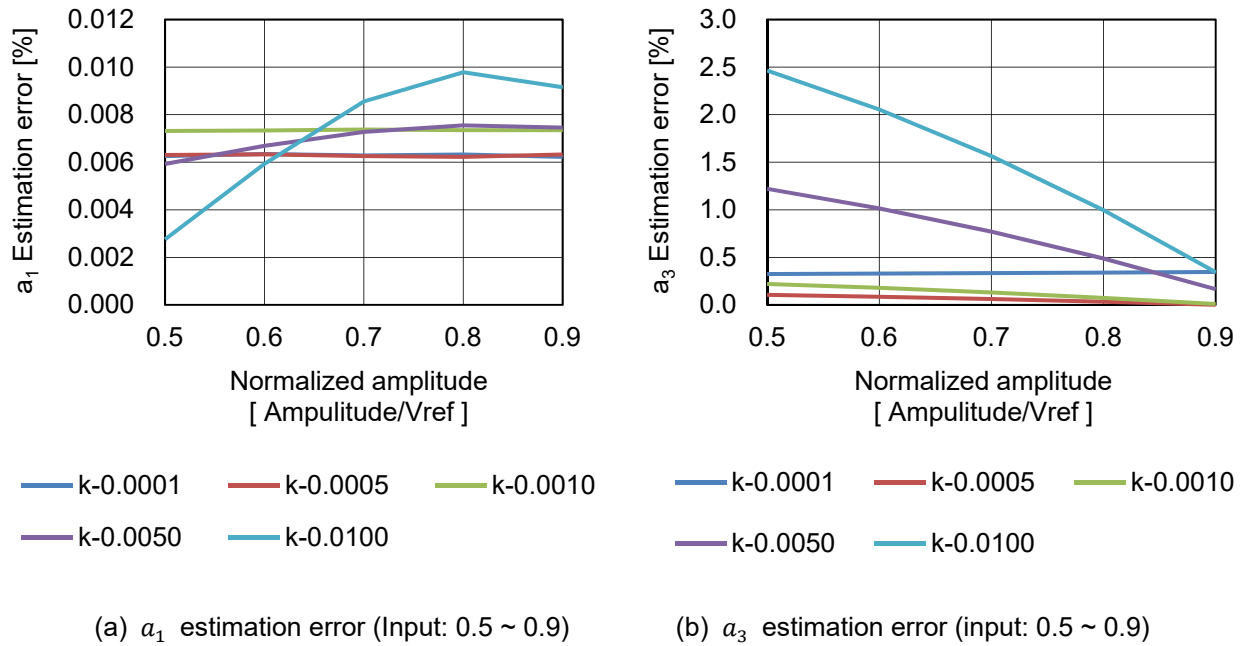


(a) $a_1$ estimation error (Input: 0.5 ~ 0.9)     (b) $a_3$ estimation error (input: 0.5 ~ 0.9)

Fig. 10. Estimation errors of the polynomial coefficients obtained from the 2nd - order modulator output power spectrum.

## 4.6 Estimation of INL with Proposed Method

In this subsection, the INL is estimated based on our prosed FFT method and compared with the reference INL obtained by the curve fitting method using simulations. We found that the amplitude 0.9 is the best value for the accurate INL estimation, and notice that during test, the input to the ΔΣADC under test can be controlled so that the input of 0.9 cos(ωt) can be provided. Table 2 shows the 3rd-order and 5th-order harmonics comparison. Fig. 11 shows their comparison for the amplitude of 0.9 when the 3rd-order harmonics is dominant (Eq. (10) is used), while Fig. 12 is the one when the 5th-order harmonics is dominant (Eq. (11) is used). The vertical axes in Fig. 11 (a), (b) and Fig. 12 (a), (b) show errors of the modulator output 1's number for $2^{20}$ data when 1LB is considered as 1/ $2^{20}$. We see in Fig. 11 (c), Fig. 12 (c) that estimated INL errors with our proposed method are sufficiently small.

Fig. 13 shows INL errors as a function of the number of the modulator output data for the amplitude of 0.9 and k=0.0005; $2^{14}$, $2^{16}$, $2^{18}$, $2^{20}$ and $2^{22}$. We see that the number of the data is larger, the error is smaller.

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Table. 2 3$^{rd}$ and 5$^{th}$ harmonics estimation maximum error.

| k | 3$^{rd}$ harmonic estimation error [%] | 5$^{th}$ harmonic estimation error [%] |
|---|---|---|
| 0.0001 | 0.0187 | 0.1421 |
| 0.0005 | 0.0213 | 0.1037 |
| 0.0010 | 0.0784 | 0.0142 |
| 0.0050 | 0.2342 | 0.0092 |
| 0.0100 | 0.4516 | 0.0276 |

## 5. Experimental Verification

We have performed experiments with a real $\Delta\Sigma$ ADC chip using the proposed algorithm. Our target INL test accuracy is within $\pm$ 1ppm, so that requirements for the input signal source are that THD < -120dB and SN > 130dB and synchronization between the signal source and the DUT (Device Under Test) of the $\Delta\Sigma$ADC in Fig. 14. Then we have developed a precise arbitrary waveform generator (AWG) whose performance is shown in Fig.15. and the NI PXI system in Fig. 16. is used and test environment in Fig. 17. The modulator output FFT results are obtained in Fig. 18, and the INL prediction is shown in Fig. 19. These results show that our proposed method can estimate the INL at ppm level.
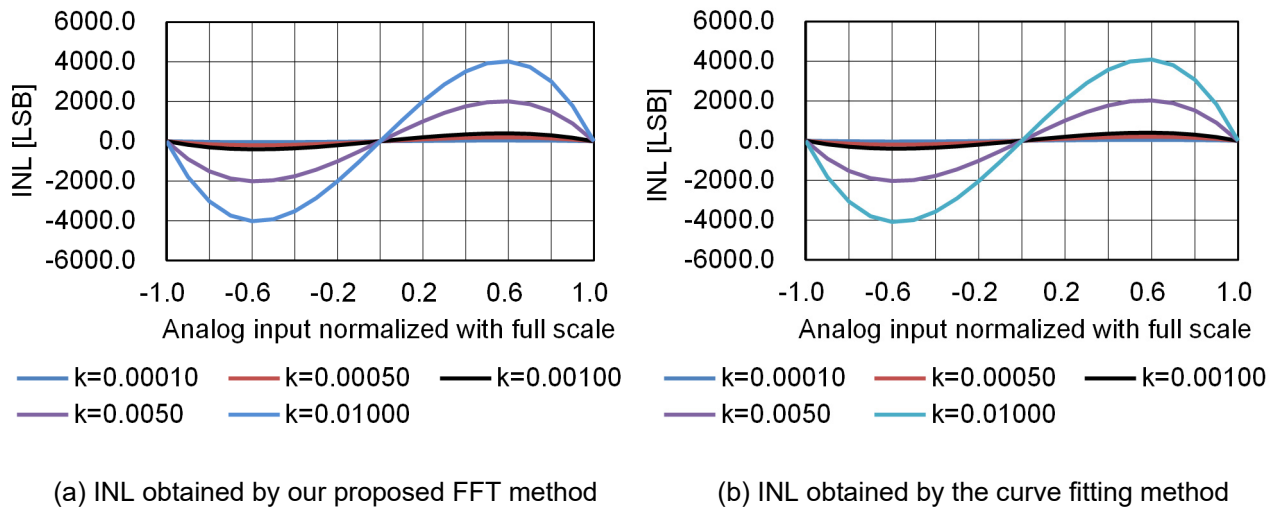


(a) INL obtained by our proposed FFT method

(b) INL obtained by the curve fitting method



(c) INL error between the FFT and curve fitting methods

Fig. 11. INL comparison between the FFT and curve fitting methods when the 3$^{rd}$-order harmonics is dominant.

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(a) INL obtained by our proposed FFT method

(b) INL obtained by the curve fitting method

(c) INL error between the FFT and curve fitting methods
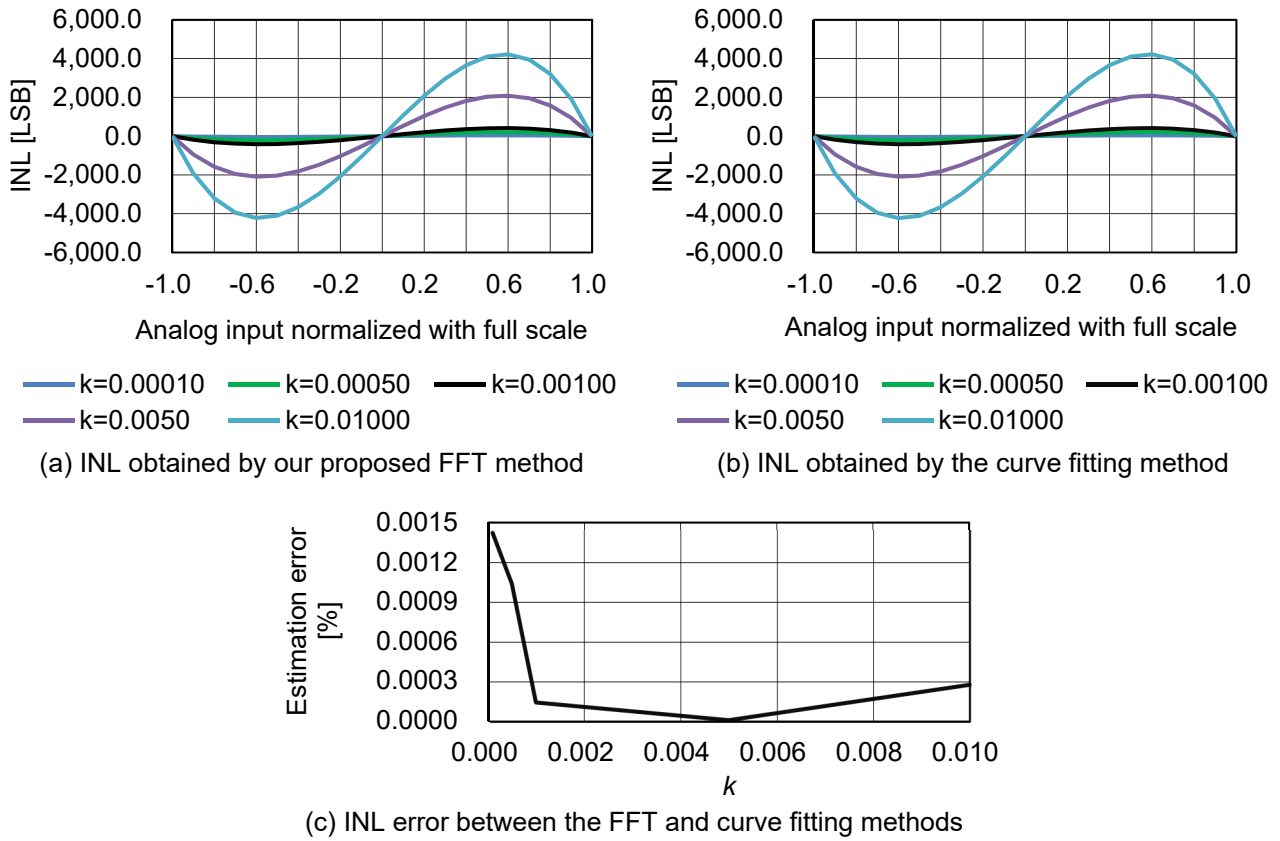
Fig. 12. INL comparison between the FFT and curve fitting methods when the $5^{th}$ - order harmonics is dominant.



(a) $a_1$ estimation error

(b) $a_3$ estimation error

(c) $a_5$ estimation error

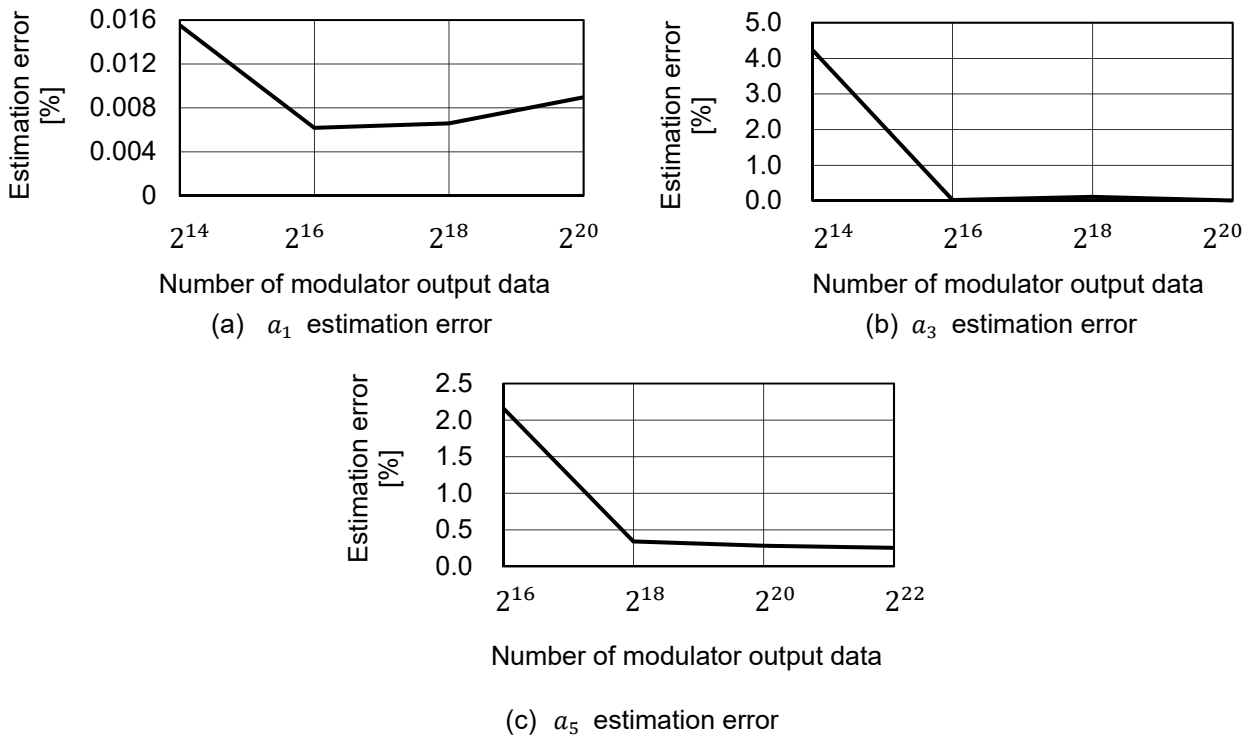Fig.13. Number of the modulator output data and estimation errors for $a_1$, $a_3$, $a_5$ with the proposed FFT method.

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FFT    CH1         VS  FREQUENCY /kHz

Output: 1kHz 44.1ksps
THD: 122dB (~5th-order harmonics)
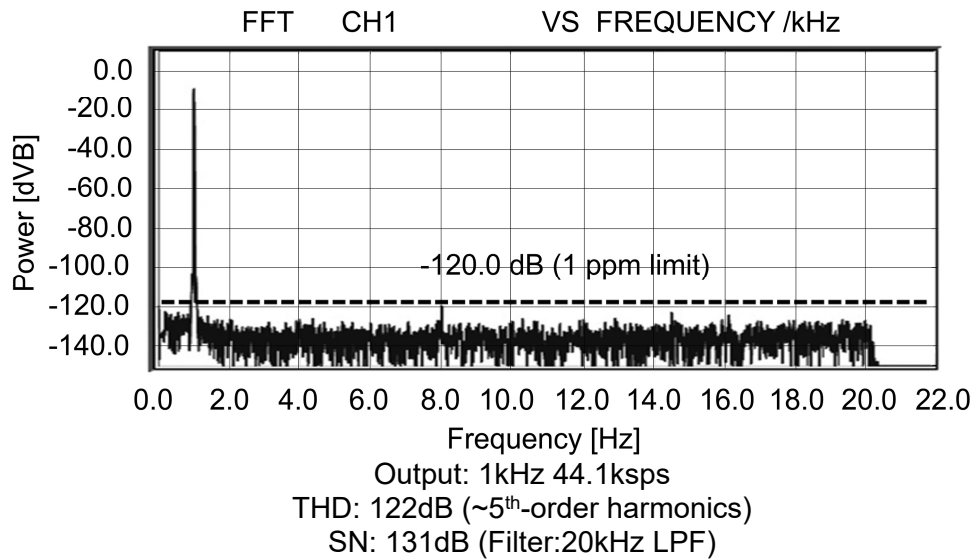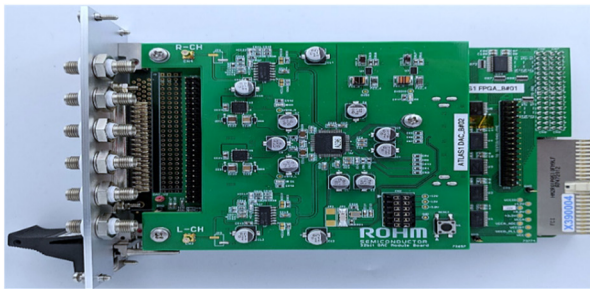SN: 131dB (Filter:20kHz LPF)

Fig. 14. Signal from our developed AWG.



(a) PXI compatible module          (b) ROHM 32bit audio DAC

Fig. 15. Development of precise AWG.



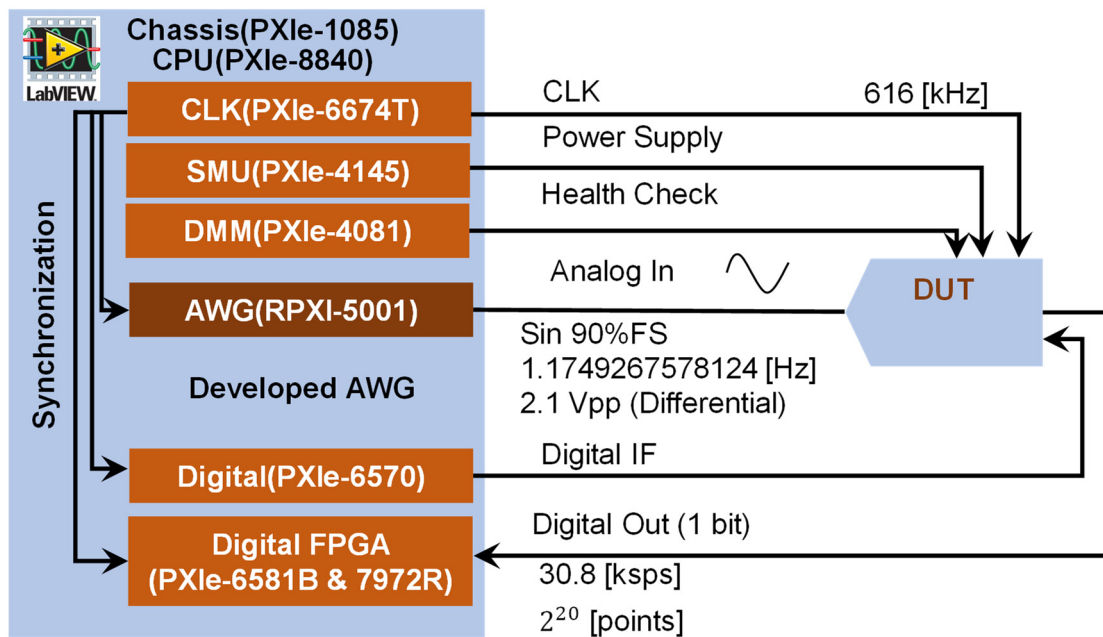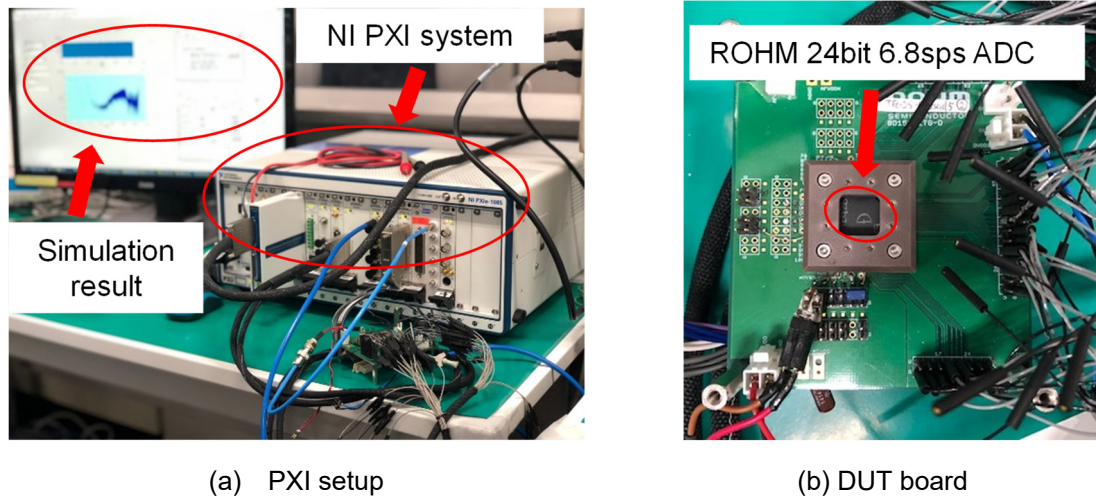Fig.16. Use of NI PXI system for experiment.

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(a) PXI setup                    (b) DUT board
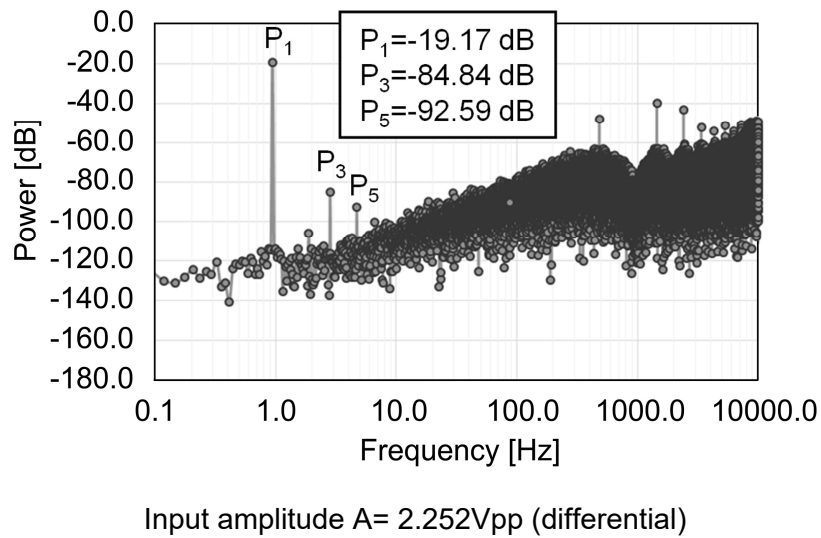
Fig. 17. Test environment.



Input amplitude A= 2.252Vpp (differential)

Fig. 18. Experimental result of the modulator output FFT.
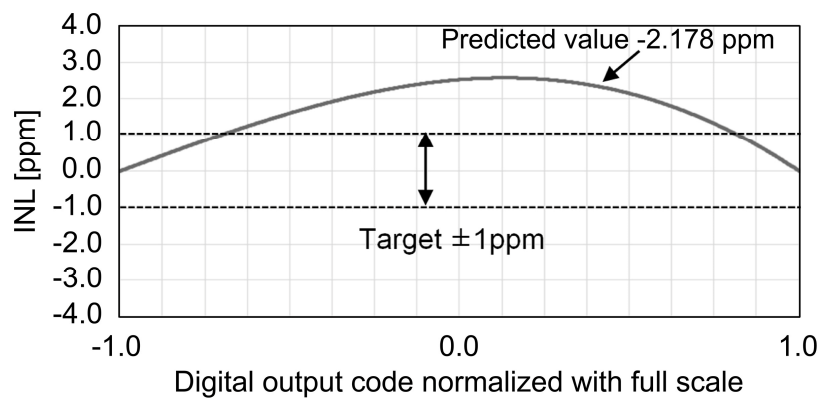


Fig. 19. Obtained INL prediction with the proposed method.

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## 6. Discussions

(i) Integral nonlinearity test time estimation:
Suppose that the $\Delta\Sigma$AD modulator operates with 32ksps and the required number of data for INL test is $2^{20}$. Then the required testing time is 32 seconds. If 32 chips are tested in parallel, the equivalent test time per chip is 1 second; this test time may be acceptable for industry applications. The following are calculation equations:

a) The INL testing time with the direct method for a 7-sps 24-bit $\Delta\Sigma$ADC is calculated by

$$\text{Test Time} = 2^{24} * \frac{1}{7} * n \text{ [sec]} = 666[\text{h}] * n \quad \text{Here, } n = \frac{\text{Samples}}{\text{Code}}$$

In case n=4, its testing time is 111 days.

b) On the other hand, when the proposed method is used, the testing time is given by

$$\text{Test Time} = 2^{20} * \frac{1}{32,000} = 32[\text{sec}]$$

(ii) One might claim that if the gain of the operational amplifier inside the modulator is not high enough, the input/output characteristics of the $\Delta\Sigma$ AD modulator can have jumps and it is not continuous [4]. However, our target $\Delta\Sigma$ ADC does not have the jumps with some circuit techniques.

(iii) For the direct INL method, a precise DC signal generator with more than 24-bit resolution is required for the modulator input. However, for the proposed method, a low distortion signal generator and a low-pass filter such as [12] are enough. Recently 32-bit $\Delta\Sigma$ ADCs are commercially announced and there would not be a DC signal generator for their INL testing with the direct method; an ultra-high-precision DC signal source is difficult to realize.

(iv) The proposed method can be applied for high-order modulators, continuous-time modulators and multi-bit modulators; this is under investigation.

(v) The proposed method can be considered as solving so-called an inverse problem. The modulator nonlinearity is modeled as a polynomial and its coefficients are estimated by the FFT method; the modulator INL is indirectly measured by its output power spectrum.

## 7. Conclusion

We have proposed a short-time high-accuracy integral linearity test method/algorithm of the high-resolution low-sampling-rate $\Delta\Sigma$ADC for mass production. We have conducted its modeling and simulation as well as experimental verification. For the next step, we will take higher-order distortions into account, and apply the proposed method to higher-order modulators. We will also perform further experiments with real $\Delta\Sigma$ADC chips and verify the test time in the ATE environment.

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