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Self-biasing Reference Current Source with Two Nagata Current Mirrors Insensitive to Temperature and Supply Voltage

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Abstract. This paper proposes a temperature and supply voltage insensitive CMOS current reference with two self-biasing Nagata current sources. They are fed-back to each other and their outputs with appropriate weights are subtracted which realizes a reference current insensitive to temperature and supply voltage. The proposed circuit is designed in TSMC 180nm process, with 3.3V supply voltage, and SPICE simulations show that it achieves a current of 22μA and its variation is less than 5% over the temperature range of -20℃ to 70℃.

1. Introduction

Current references are one of the key building blocks in analog circuits such as amplifiers, oscillators and data converters [1]. Moreover, a reliable reference current independent of process, supply voltage and temperature (PVT) variation is a necessity for designing analog ICs. The bandgap reference circuit is widely used. It sums the negative and positive temperature coefficients voltages or currents generated by the base-emitter voltage (V_{be}) and ΔV_{be} of the BJT, and the reference voltage or current is obtained [4,5]. But the conventional bandgap reference needs (parasitic) bipolar transistors and an operational amplifier which increase chip area and power. For a low power dissipation and nano-ampere current, references consisting of MOS transistors operating in subthreshold region are presented in [6, 7]. One of the widely used current reference circuits is the peaking current mirror invented by Minoru Nagata in 1966 [1-3], referred to as the Nagata current mirror; it is mainly used as a supply voltage insensitive reference current source with simple configuration. Its several modified circuit topologies have been reported [11-14].

In this paper, we consider a reference current source which uses PMOS-type and NMOS-type Nagata current sources that are fed-back to each other with self-biasing configuration for supply voltage insensitivity; to achieve temperature insensitivity, their output current difference with

appropriate weighting is obtained by a subtraction circuit. SPICE simulations assuming TSMC 0.18μm CMOS parameters verify its performance. Here, we do not consider the absolute value of the output current, only its temperature and supply voltage independence.

Section 2 details an analysis of the conventional Nagata current mirror, and Section 3 describes the proposed circuit with simulation results. Section 4 shows its comparison with other works and Section 5 provides conclusion.

2. Analysis of Nagata Current Mirror Circuit

The Nagata current mirror has nonlinear input-output current characteristics (Figs. 1, 2); it has a peak with respect to the supply voltage (or the input current) change [1-3]. We start by deriving the mathematical relationship between the input and output currents.

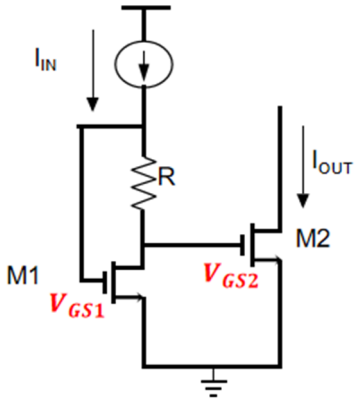


Fig. 1. Nagata current mirror.

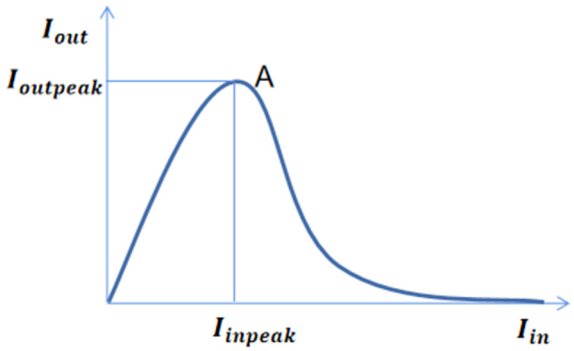


Fig. 2. I-O current characteristics of Nagata current mirror.

It follows from the Kirchhoff voltage law that

$$V_{GS1} = V_{GS2} + RI_{in} \tag{1}$$

Assuming that the drain currents of M1 and M2 follow the square law in the saturation region, and ignoring the channel length modulation effect for simplicity, we have the following:

$$I_{in} = K_1(V_{GS1} - V_t)^2 \tag{2}$$

$$I_{out} = K_2(V_{GS2} - V_t)^2 \tag{3}$$

Here $K = {}^{1}/_{2}\,\mu_n C_{ox}\frac{W}{L}$. μ_n is the electron mobility, C_{ox} is the unit capacitance of gate, (W/L) is an aspect ratio of the MOSFET.
The gate-source voltages V_{GS1}, V_{GS2} of M1, M2 can be derived as

$$V_{GS1} = \sqrt{\frac{I_{in}}{K_1}} + V_t \tag{4}$$

$$V_{GS2} = \sqrt{\frac{I_{out}}{K_2}} + V_t \tag{5}$$

Substituting Eq. (4) and Eq. (5) into Eq. (1) yields the output current as

$$I_{out} = K_2 R^2 \left(\sqrt{\frac{I_{in}}{K_1 R^2}} - I_{in}\right)^2 \tag{6}$$

To find the maximal value of the output current in Fig.2, we differentiate I_{out} with respect to I_{in}, and write the result as:

$$\frac{dI_{out}}{dI_{in}} = 2K_2 R^2 \left(\sqrt{\frac{I_{in}}{K_1 R^2}} - I_{in}\right)\left(\sqrt{\frac{1}{K_1 R^2}} \times \sqrt{\frac{1}{4I_{in}}} - 1\right) \tag{7}$$

When $\frac{dI_{out}}{dI_{in}} = 0$, we obtain the following:

$$I_{in1} = \frac{1}{K_1 R^2} \tag{8}$$

$$I_{in2} = \frac{1}{4K_1 R^2}\ . \tag{9}$$

I_{in2} is the value we need. Substituting it into Eq. (6) gives the maxima value of the output current as:

$$I_{out} = \frac{1}{16K_1 R^2} \times \frac{K_2}{K_1}\ . \tag{10}$$

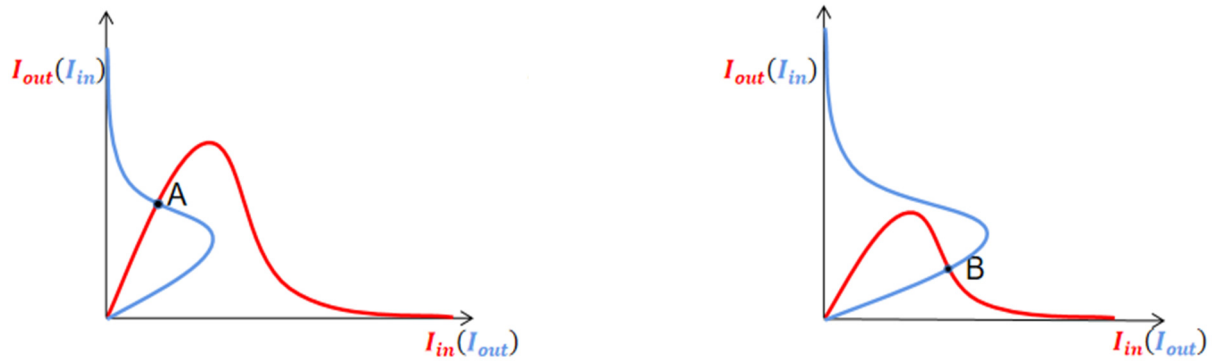
The equation above shows that the output current can be changed by adjusting resistor value and MOSFET size.

3. Proposed Reference Current Source

3.1 Two Nagata Current Source Circuits Fed-back Each Other with Self-Bias Configuration

As mentioned above, the output current has a monotonically increasing property before reaching its peak and reverses after crossing the peak. To achieve a stable output current, the circuit should operate under negative feedback. That is, we can make the upper and lower current mirrors have different monotonic properties by setting the appropriate resistance values and MOSFET sizes.

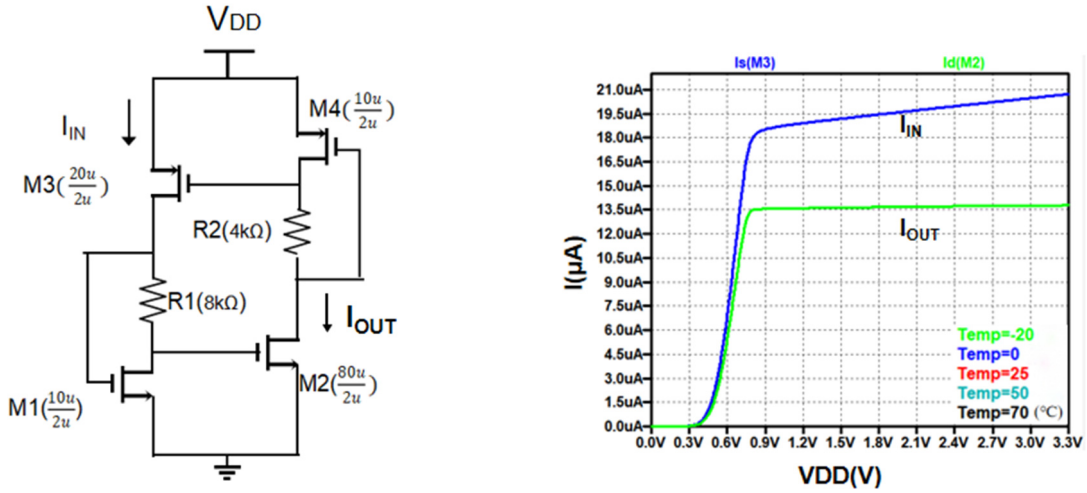
As shown in Fig. 3 and Fig. 4, we make a resistor R_1 bigger or smaller than R_2 to make the circuit operate at point B or A which ensures negative feedback operation. Thus, the circuit can output a stable current. Here we chose point B; it means the output current of lower current mirrors has monotonically decreasing properties [8-10]. Fig. 5 shows simulated gate-source and drain-source voltages of M2 and I_{OUT} while Fig. 6 shows source-gate and source-drain voltages of M3 and I_{IN}. In Fig. 5, because the lower Nagata current mirror has monotonic decreasing property (Fig. 3 (b) red line), a slight decrease in V_{GS} for M2 makes its drain current insensitive to the supply voltage although V_{DS} increases. On the other hand, the output current of M3 increases slightly as a result of the channel length modulation effect, because the upper Nagata current mirror is biased to have monotonically increase property (Fig. 3 (b) blue line).



(a) The upper Nagata current mirror is in monotonically decreasing state while the lower is in decreasing state

(b) The upper is in increasing sate while the lower is in decreasing state

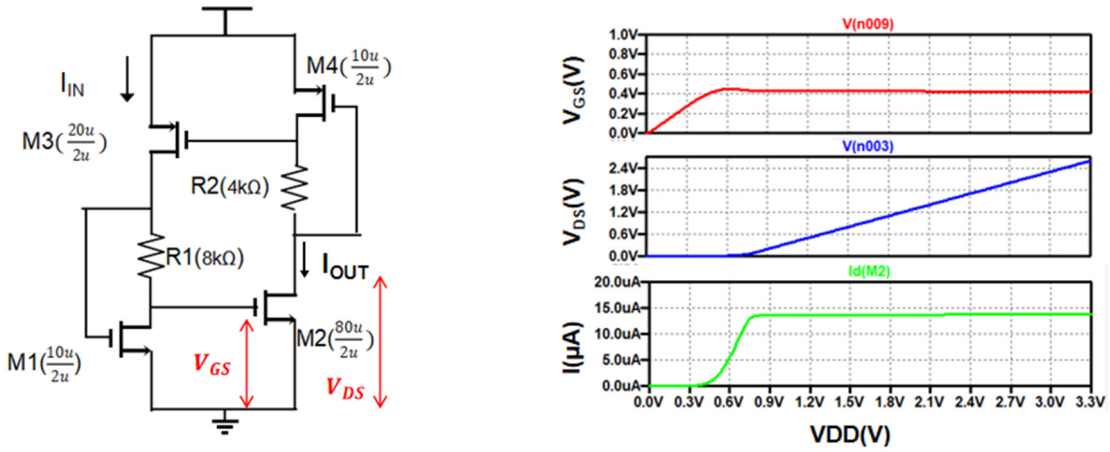
Fig. 3. Input-output current characteristics of Nagata current sources.



(a) Investigated circuit

(b) Simulation results

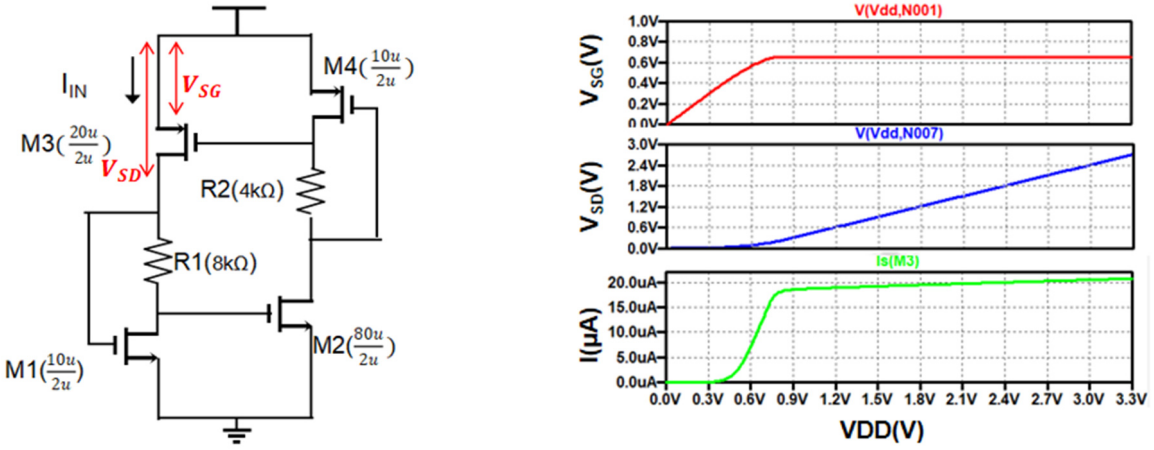
Fig. 4. Investigated self-biasing Nagata current mirror circuit and SPICE simulation results.



(a) Investigated circuit

(b) Simulation results of M2

Fig. 5. Gate-source and drain-source voltages of M2.

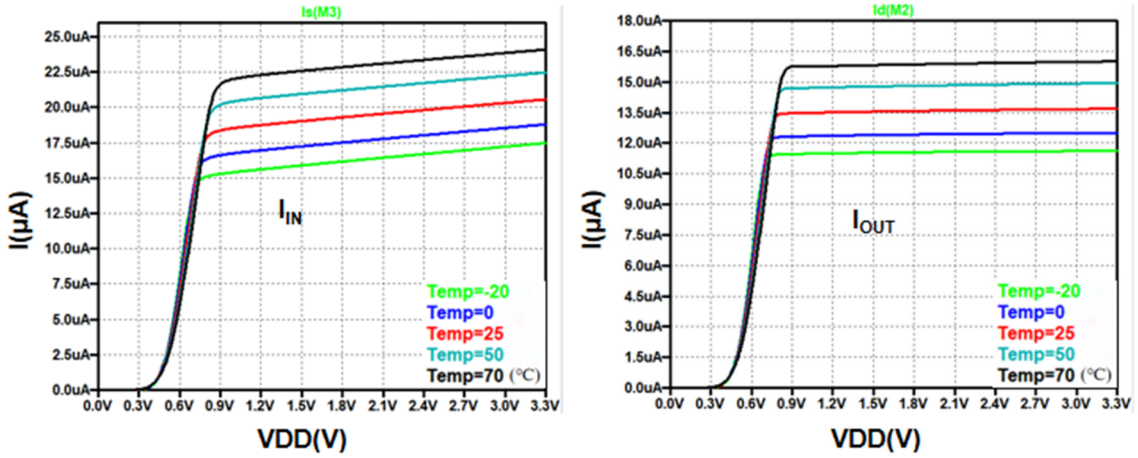


(a) Investigated circuit (b) Simulation results of M3

Fig. 6. Source-gate and source-drain voltages of M3.

3.2 Subtraction Circuit

Although we already have a supply voltage insensitive output current as shown in Fig. 4, it remains temperature sensitive (Fig. 7). Since I_{IN} and I_{OUT} both increase when temperature increases, we can take a subtraction operation to cancel the temperature dependency.



(a) I_{IN} with respect to V_{DD} (b) I_{OUT} with respect to V_{DD}

Fig. 7. Input and output currents with temperature change.

We see in Fig. 4 that the input current is larger than the output current and slightly depends on the supply voltage; the output current remains insensitive to the supply voltage. So we amplify one output current to I_2 and reduce the other one to I_1 (Fig. 8). The difference current (I_3) between the two currents (I_1, I_2) flows through M7 and is insensitive to temperature. Re-amplifying it by M8 yields the desired value needed, I_{OUT}.

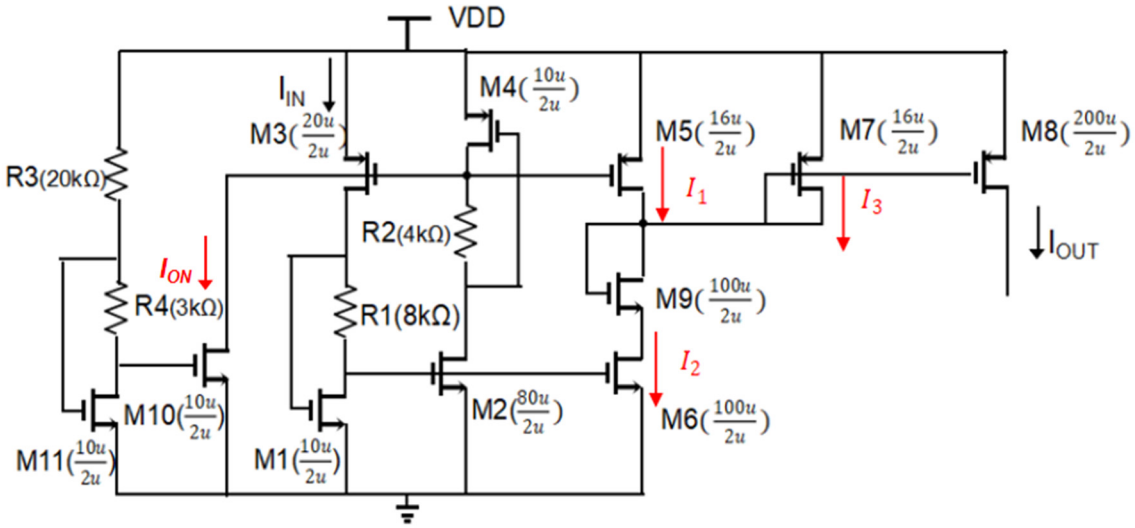
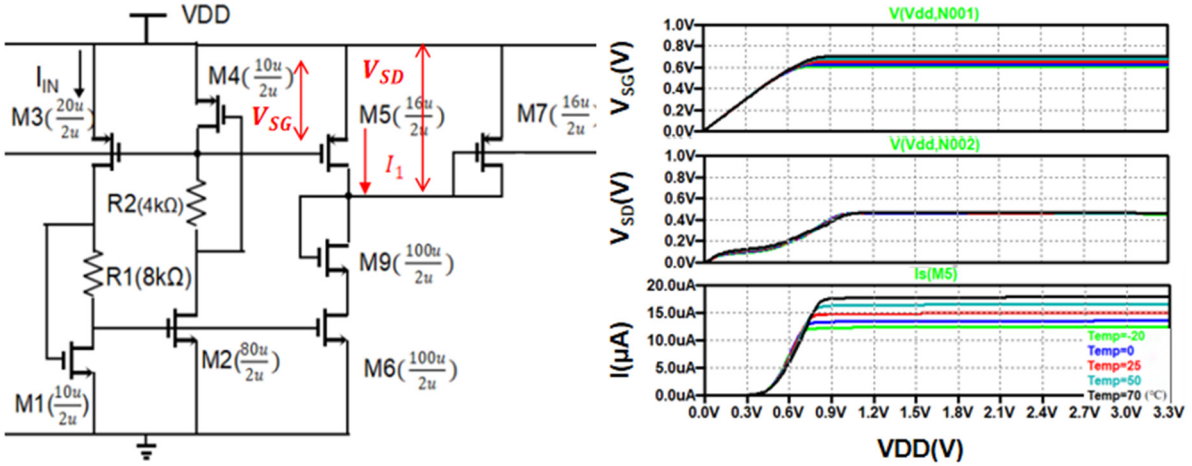
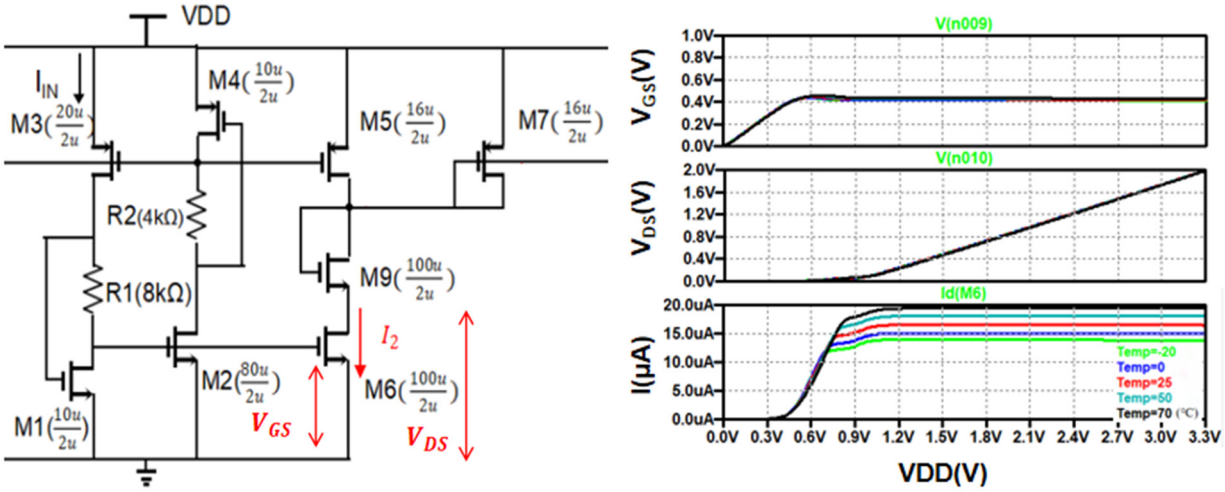


Fig. 8. Proposed reference current source with subtraction circuit and start-up circuit.



(a) Proposed circuit (b) Simulation results of M5

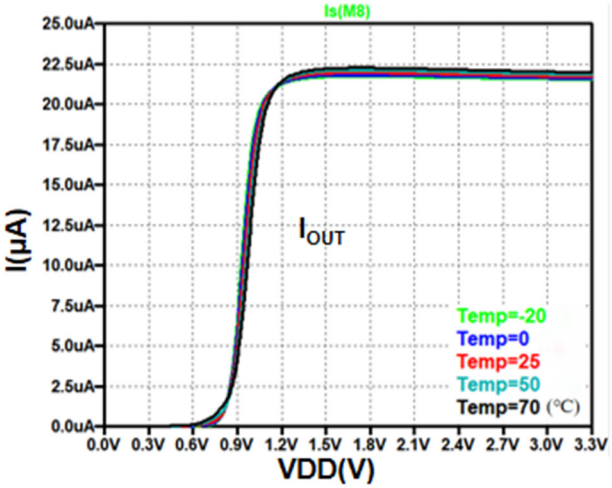
Fig. 9. Source-gate and source-drain voltages of M5 with respect to V_{DD}.



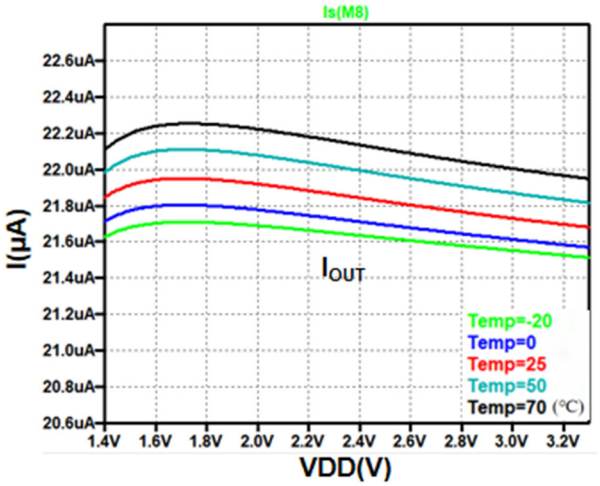
(a) Proposed circuit (b) Simulation results of M6

Fig.10. Gate-source and drain-source voltages of M6 with respect to V_{DD}.

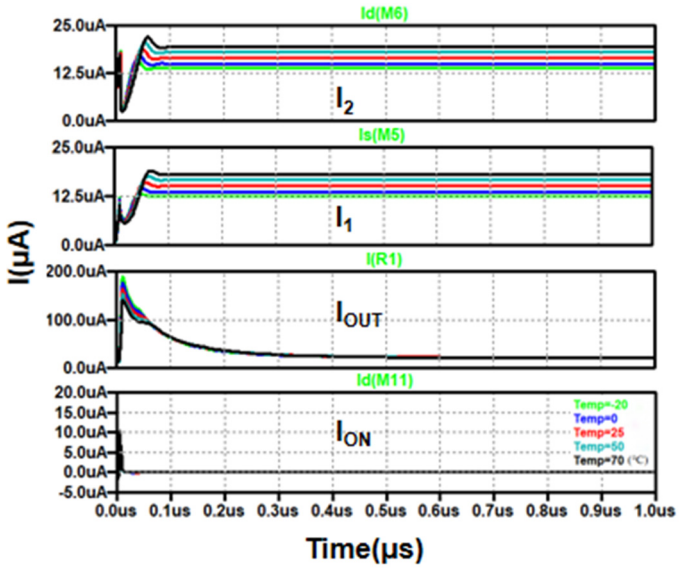
Fig. 9 shows that in the subtraction circuit, V_{SD} of M5 becomes constant with respect to supply voltage V_{DD}, which is different from M3, and hence current I_1 is insensitive to V_{DD}. Fig. 10 shows that the slight decrease in V_{GS} and increase in V_{DS} for M6 with respect to an increase in V_{DD} makes current I_2 insensitive to V_{DD}.



(a) I_{OUT} with respect to VDD



(b) I_{OUT} with respect to VDD between 1.5V-3.3V



(c) Transient simulation result of the whole circuit.

Fig. 11. Simulated output current of the reference source circuit in Fig. 8.

When V_{DD} rises, M10 and M11 turn on. The current flowing through M10 and M11 increases, which causes the gate potential of M3 to decrease. At a certain time, M3 turns on, which makes M1, M2 and M4 turn on in order so the whole circuit starts to work. As the current keeps increasing, the gate voltage of M10 becomes lower than its threshold voltage, which makes it turn off. We see in Fig. 11 that the circuit operates properly with the startup circuit when V_{DD} rises from zero to 3.3V in 0.5μs. By appropriately setting the sizes of the MOSFETs in the subtraction circuit, the temperature dependency error is well cancelled; the output current has about 0.55uA error (2.5 % error) over the temperature range of -20℃ to 70℃ at 1.8V, and 0.3uA error (1.4 % error) with the supply voltage change between 1.5V to 3.3V.

4. Comparison With Other Works

We have compared the proposed circuit with other existing designs in Table 1; it shows that the proposed current reference can work at a wide voltage. As the Nagata current source is compact, it is easy to realize supply voltage independent by using two self-biased Nagata current sources. The original Nagata current source does not care for the temperature variation, but the proposed Nagata current source suppresses the temperature variation dependency to some extent, though it may not be well insensitive to temperature. Also, its structure is not complicated and does not use an operational amplifier.

Table 1 Comparison of the proposed circuit with other design works

	This Work	[4]	[5]	[6]	[7]
Technology	**180nm**	500nm	180nm	350nm	180nm
Supply Voltage[V]	**1.5~3.3**	1.8	2.4~3.0	1.8~3.0	1.25~1.8
Reference Current	**22μA**	7.25μA	10μA	96nA	92.3nA
Temp Co. [ppm/℃]	**277**	0.7	130	520	177
Temp Range [℃]	**-20~70**	-20~150	-40~80	0~80	-40~85

5. Conclusion

This paper has proposed a CMOS reference current source with two Nagata current mirror circuits that are fed-back to each other. Immunity to supply voltage change is realized using a self-basing configuration while temperature insensitivity is realized by subtraction of the two Nagata current source outputs with appropriate weighting. Our SPICE simulation results with TSMC 0.18μm CMOS parameters showed its effectiveness. One advantage of our proposed circuit is that it does not need positive temperature coefficient resistors for realizing temperature insensitivity.

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