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Comparison of Three Types of Startup Circuits for a Self-Biasing MOS Reference Current Source

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Abstract. This paper studies three startup circuits for use in our self-biasing reference current source. First, we present our proposed self-biased MOS reference current source, which is designed on TSMC 0.18μm BSIM3v3 CMOS SPICE parameters. LTspice simulations show that its output current is insensitive to temperature. Since it has two stable states, a startup circuit is required for its proper operation, i.e., a finite current flow. Therefore, we compare the three circuits in terms of chip area, power consumption, and startup operation reliability. We clarify their pros and cons, and show a guideline for selecting the startup circuit best suited for a specific application of the reference current source circuit.

1. Introduction

In many cases, an analog IC requires a temperature-independent reference current or voltage source [1, 2]. In this paper, we introduce a Gunma University (GU) reference current source [3] as well as its self-biasing function and startup circuit. The temperature insensitivity of its drain current is realized by setting the gate voltage of the MOSFET to an appropriate value. This circuit has two stable states: one in which some current flows and the other in which no current flows. Thus, the startup procedure must force some amount of current to flow and induce the former state [4]. In this paper, three types of typical startup circuits are studied and compared in terms of chip area, power consumption, and startup operation reliability. There are many startup circuits already published [5-14]; most of recent ones are for low supply voltage and low power operation.

Section 2 shows the NMOSFET drain current (I_{DS}) temperature characteristics in details, while Section 3 shows SPICE simulation results of a Gunma University (GU) reference current source. Section 4 describes the operation of the three types of startup circuits and compares their advantages and disadvantages. Section 5 provides our conclusions.

2. Drain Current Temperature Characteristics of MOSFET

The simulations in this paper assume TSMC 0.18μm BSIM3v3 CMOS SPICE parameters. Fig. 1 shows the relationship between the gate-source voltage (V_{GS}) and the drain current (I_{DS}) of an NMOSFET. By setting the gate voltage to V_{CP} (cross point gate voltage), the drain current becomes insensitive to temperature. At gate voltages higher than V_{CP}, the drain current increases at low temperature, whereas at gate voltages lower than V_{CP}, the drain current increases at high temperature [15].

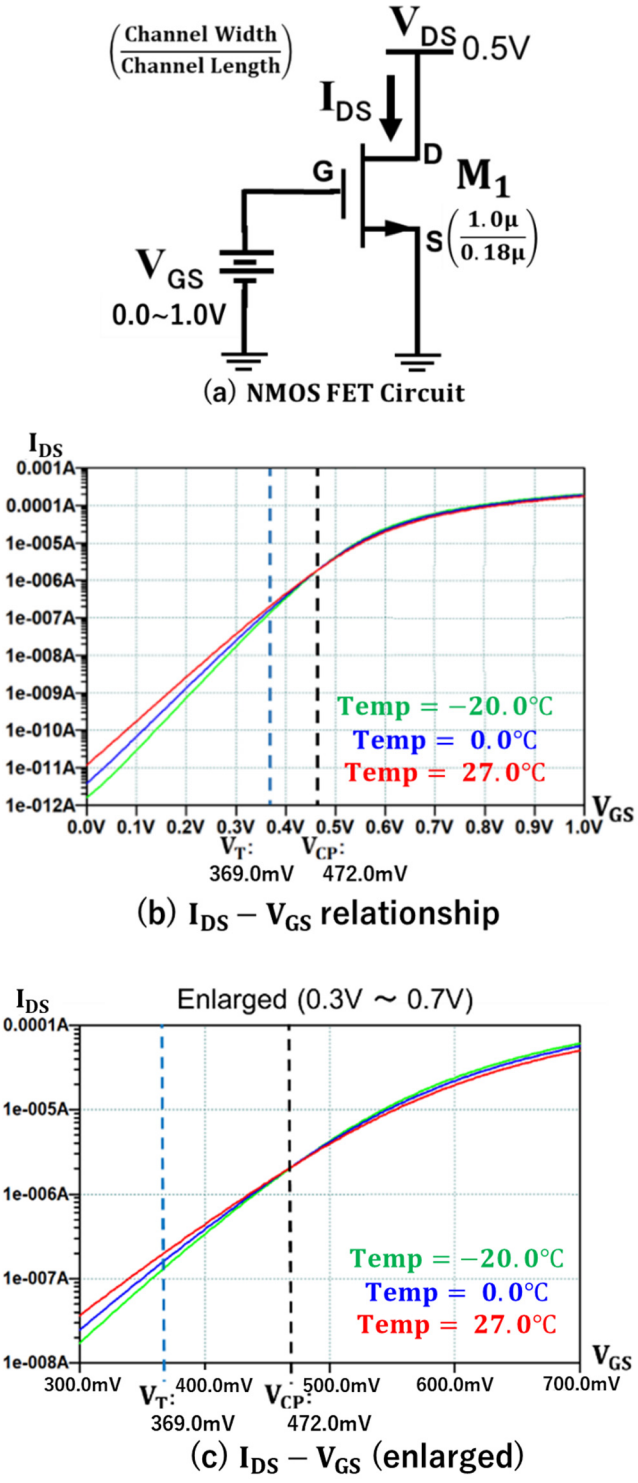

Fig. 1. Drain current temperature characteristics of NMOSFET.

3. Gunma University (GU) Reference Current Source

Fig. 2 shows our proposed MOS reference current source (Gunma University (GU) reference current source). We previously proposed this circuit in reference [16]. The structure of the circuit in Fig. 2 of this paper and the circuit proposed in reference [16] are the same. On the other hand, in reference [16], we did not determine specific values for MOS and resistor values, but in this paper, we have determined these values. In the stable state, the gate-source voltage of M_{N4} (V_2) is higher than V_{CP}, whereas the gate-source voltages of $M_{N2,5\sim9}$ (V_2-V_4) are lower than V_{CP}. Since I_3 is the sum of M_{N4} and $M_{N2,5\sim9}$ drain currents, the temperature characteristics of the current are cancelled. I_3 is mirrored by the PMOS cascode current mirror circuit (M_{P2}, M_{P5}, M_{P3}, M_{P6}) and I_{OUT} is provided as the output current.

Similarly, I_3 is mirrored by the PMOS cascode current mirror circuit (M_{P2}, M_{P5}, M_{P1}, M_{P4}), and I_1 is injected into the gate voltage generator circuit. However, as I_1 increases, the gate voltage of M_{N4} and M_{N2} increases, and I_3 further increases, which causes a positive feedback effect and makes the circuit unstable. As shown in Fig. 3, when I_1 increases, the gate voltages of M_{N3} and M_{N1} also increase, which makes I_2 increase and I_1 decrease. As a result, the increases of M_{N4} and M_{N2} gate voltages can be suppressed and they become stable. Design for this negative feedback action and design of temperature insensitivity of I_2 and I_3 are important in this circuit.

This self-biasing can be achieved by carefully designing the values of R_1 and R_2, and the sizes of M_{N3} and M_{N1}. The gate lengths of M_{N3} and M_{N1} are designed to be large enough so that the drain current is proportional to the square of (V_2-V_T) and ((V_2-V_1)-V_T), to support self-biasing. The combined drain currents of M_{N3} and M_{N1} realize temperature insensitivity. Here V_T is the threshold voltage of the NMOSFET.

Notice that since this circuit has two stable states, a startup circuit is needed to force it to operate in the desired state (current flowing state).

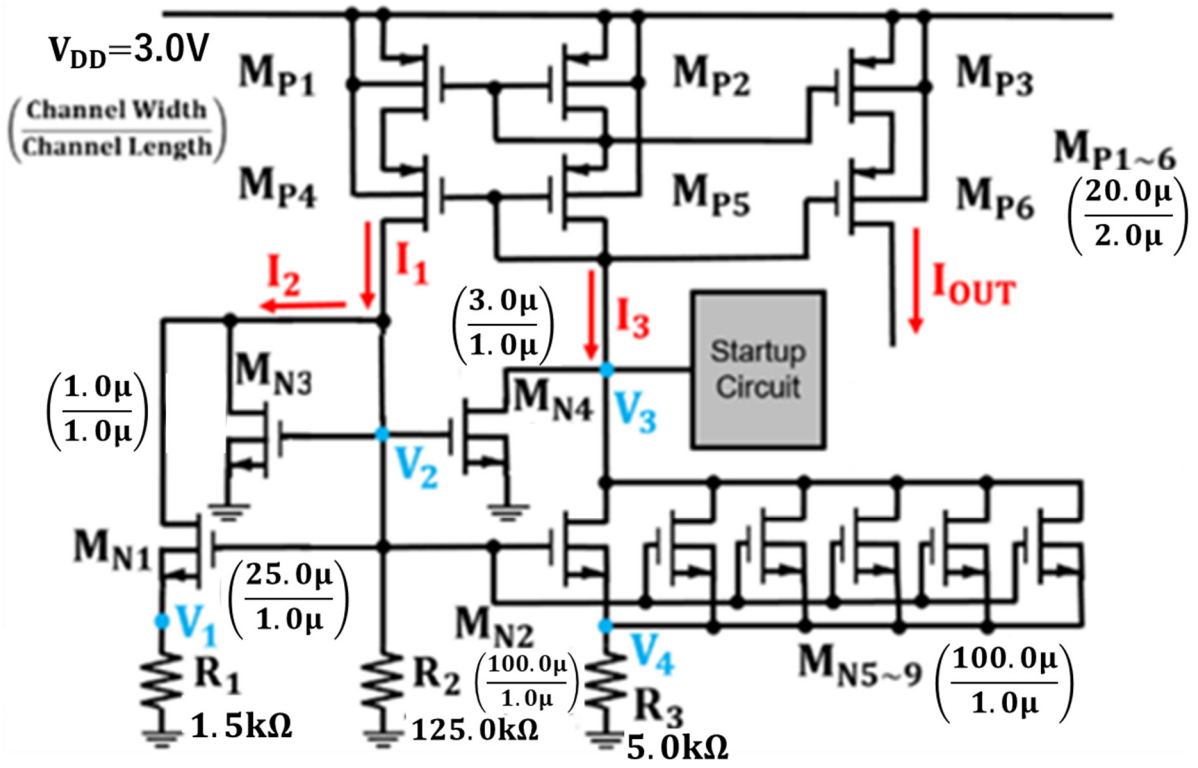

Fig. 2. Self-biasing MOS reference current source.

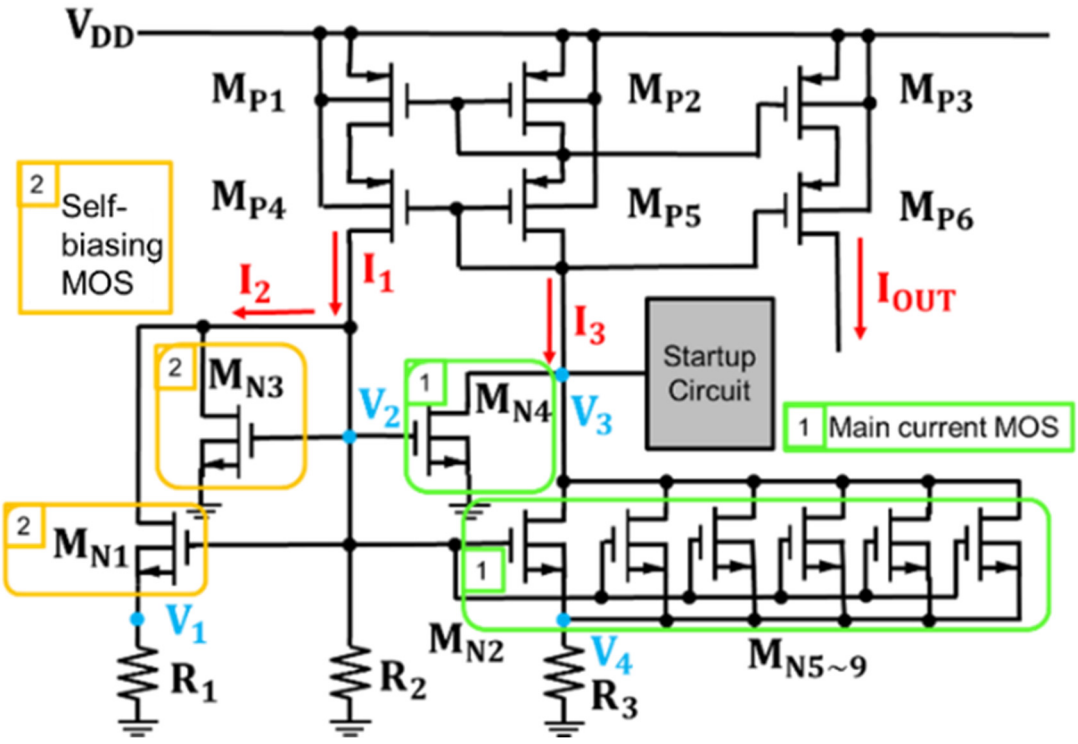

Fig. 3. V_2 suppression by self-biasing MOS.

Fig. 4 shows the output current I_{OUT} of the proposed circuit in Fig. 2. Here, the reference temperature is 27°C. In the temperature range of -30°C to + 80°C, output current fluctuations or relative errors are less than 0.7 [%]. The relative error in Fig. 4 is defined as the difference between the output current at 27°C ($I_{OUT(27°C)}$) and the one at p°C ($I_{OUT(p°C)}$) as follows:

$$\text{Error (p°C)} = \left(\frac{I_{OUT(p°C)} - I_{OUT(27°C)}}{I_{OUT(27°C)}}\right) * 100[\%] \quad (1)$$

Fig. 5 shows the gate-source voltages of M_{N2} and M_{N4} for the GU reference current source circuit of Fig. 2. The gate-source voltage of M_{N4} is higher than V_{CP} and that of M_{N2} is lower than V_{CP}.

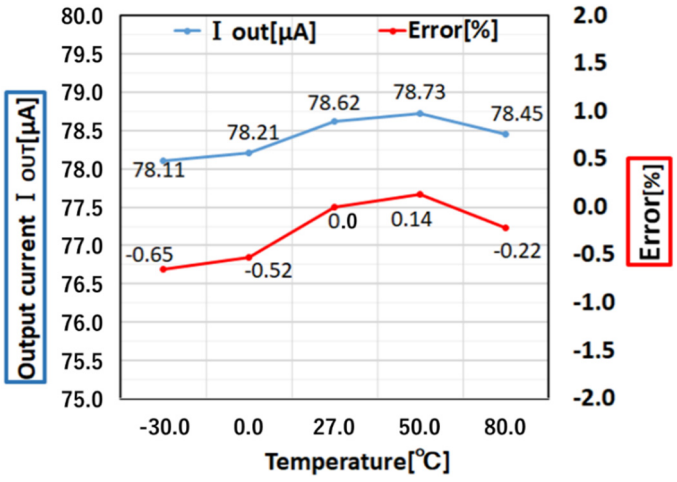

Fig. 4. Output current of the proposed circuit and error from the current at 27°C.

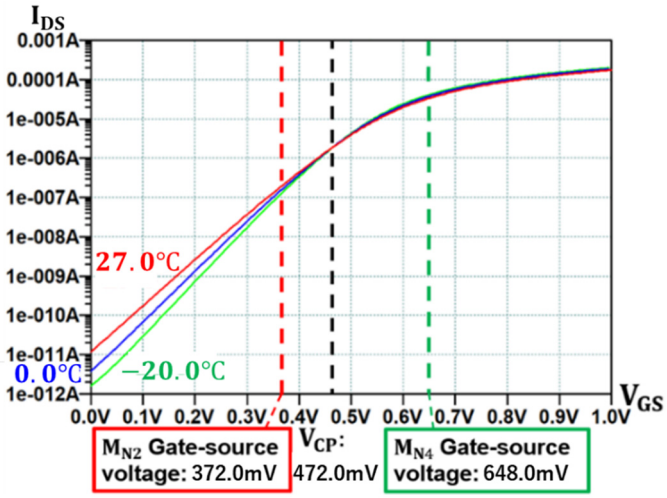

Fig. 5. Gate-source voltages of M_{N2} and M_{N4} (threshold voltage of 369 mV).

In Fig. 5, the red line indicates I_{DS} at 27°C, the blue line at 0°C, and the green line at -20°C. The green vertical dotted line shows the gate source voltage of M_{N4}, and the red one expresses that of M_{N2}, while the black one indicates V_{CP}. Since the gate-source voltage of M_{N4} is higher than V_{CP}, more current flows at lower temperatures, and that of M_{N2} is lower than V_{CP}, more current flows at high temperature. The graph in Fig. 5 is for W/L = 1μm/0.18μm so that it does not match the one in Fig. 2; this graph is used to show the relationship among the gate-source voltages of M_{N4}, M_{N2} and V_{CP}.

4. Three Startup Circuits

This section describes three types of startup circuits for the GU reference current source. A self-biasing reference current source circuit has a proper stable operating point A that yields the desired reference current, and an erroneous stable point B yielding no current. Therefore, a startup circuit is used to enforce operating point A.

4.1 Startup Circuit 1

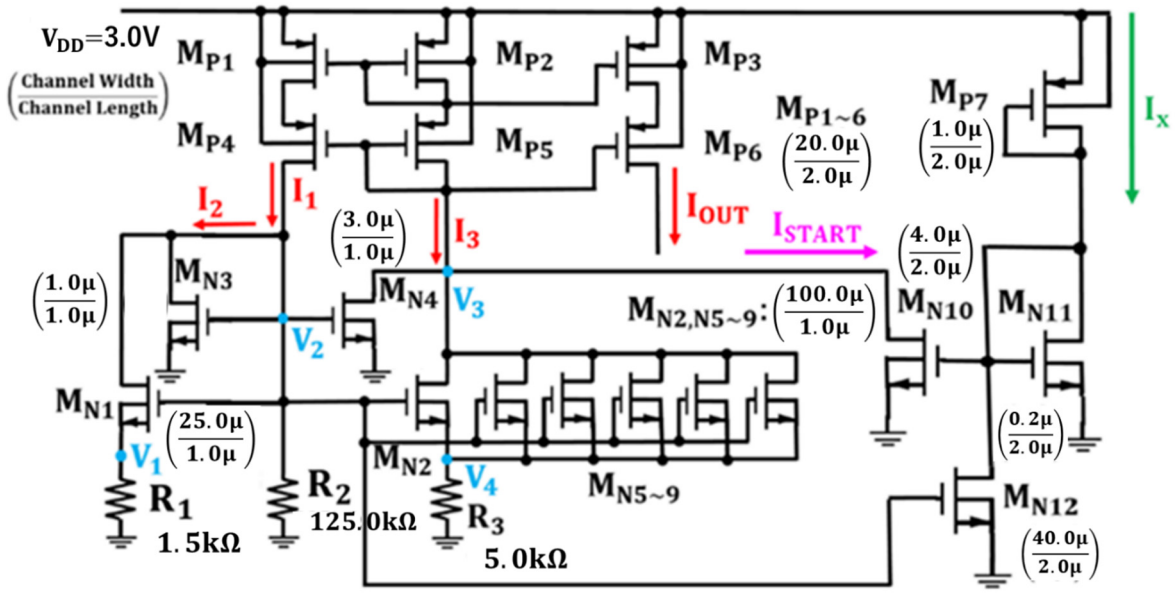

Fig. 6. GU reference current source with startup circuit 1.

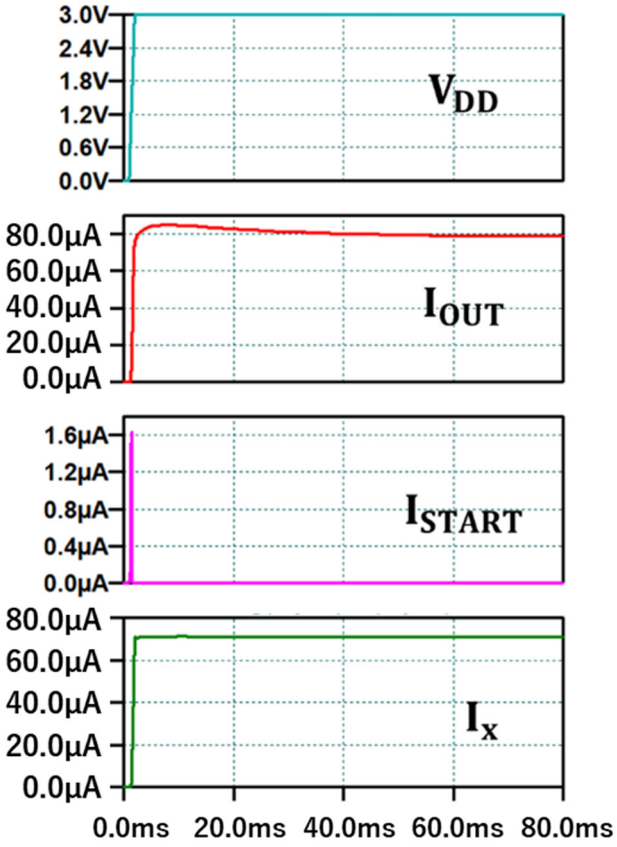

Fig. 7. Simulation results at 27°C.

The startup circuit of Fig. 6 operates as follows:

1) Before the power turns on, all node voltages are 0V. At startup, V_{DD} starts to increase, M_{P7} turns on, the gate voltages of M_{N10} and M_{N11} increase, and M_{N10} turns on.
2) The startup current flows through M_{P2}, M_{P5}, and M_{N10} to GND. Due to the PMOS cascode current mirroring, the same amount of current flows through M_{P1} and M_{P4}.
3) The gate voltages of $M_{N2,N5\sim9}$ and M_{N4} increase, and they turn on. Therefore, the current flows along the paths of M_{P2}, M_{P5}, and $M_{N2,N5\sim9}$.
4) As the gate voltage of $M_{N2,N5\sim9}$ increase, the gate voltage of M_{N12} also increases, so that M_{N12} turns on. Eventually, the gate voltage of M_{N10} drops to a low voltage and it turns off; the operation as a startup circuit stops.
5) After that, the current continues to flow through M_{P7} and M_{N12} to GND, and M_{N10} remains off.

We see from Fig. 7 that current I_X flows through M_{P7} even after the startup operation completes and the normal operation commences. This non-zero (finite) steady current is a problem. Startup circuit 2 attempts to alleviate this problem.

Notice that a similar start-up circuit is described in [2], which has no bias current after start-up operation, but it may be difficult to design the MOSFET sizes for proper operation depending on the self-bias core circuit.

4.2 Startup Circuit 2 (CMOS inverter usage)

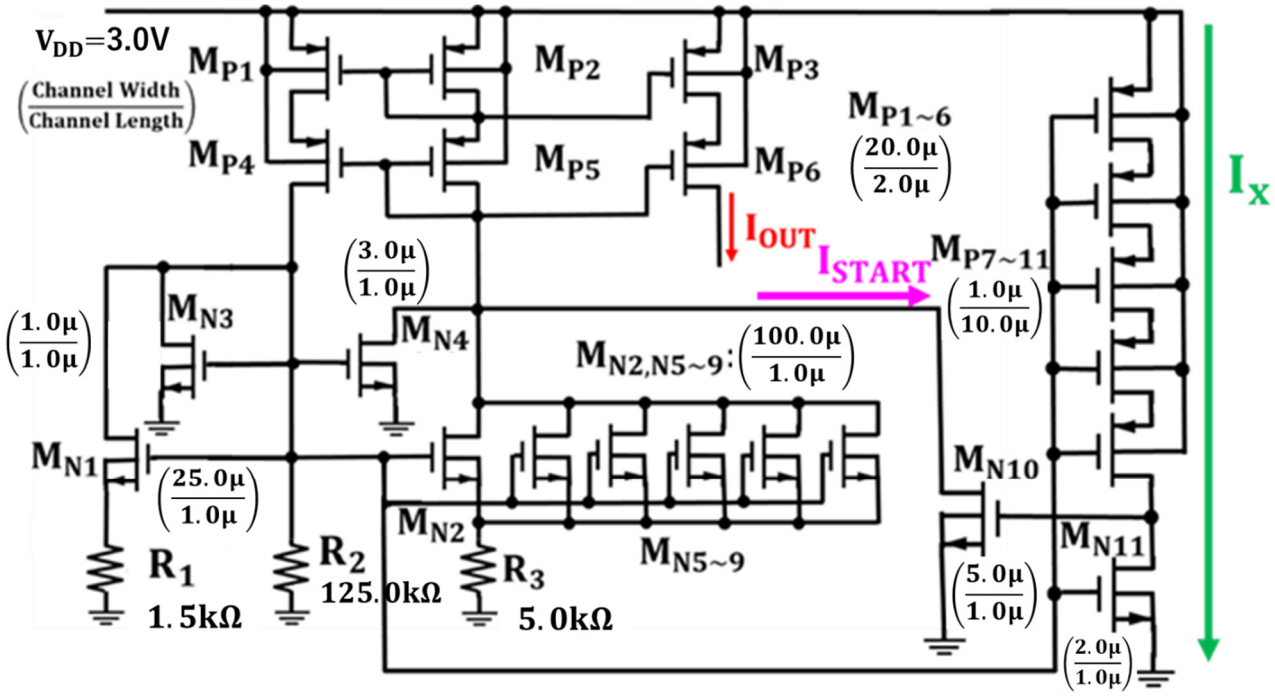

Fig. 8. GU reference current source with startup circuit 2.

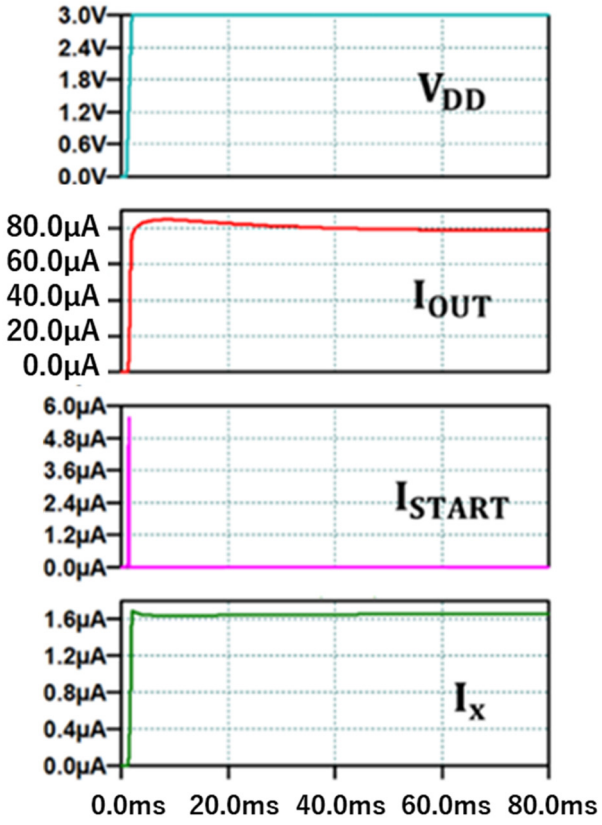

Fig. 9. Simulation result at 27°C.

The startup circuit of Fig. 8 operates as follows:

1) Before the power turns on, all node voltages are 0V. At startup, V_{DD} starts to increase, $M_{P7\sim11}$ turn on, the gate voltage of M_{N10} increases, and M_{N10} turns on.
2) The startup current flows through M_{P2}, M_{P5}, and M_{N10} to GND. Due to the PMOS cascode current mirroring, the same current flows through the paths of $M_{P1}$and M_{P4}.
3) The gate voltages of $M_{N2,N5\sim9}$ and M_{N4} increase, and they turn on. Therefore, the current flows along the paths of M_{P2}, M_{P5}, and $M_{N2,N5\sim9}$.
4) As the gate voltages of $M_{N2,N5\sim9}$ increase, the gate voltages of $M_{P7\sim11}$, and M_{N11} also increase, so that $M_{P7\sim11}$ turn off and M_{N11} turns on. Eventually, the gate voltage of M_{N10} drops to GND and it turns off; the operation as a startup circuit stops.

We see from Fig. 9 that by suppressing current I_X, the power consumption is suppressed compared with startup circuit 1. However, current I_X is still flows. In addition, a larger number of MOSFETs are required than startup circuit 1, which increases the chip area. Startup circuit 3 suppresses current I_X by using a capacitor.

4.3 Startup Circuit 3 (Capacitor usage)

The startup circuit of Fig. 10 operates as follows:

1) Before the power turns on, all node voltages are 0V. At startup, V_{DD} starts to increase, capacitor C_1 charges, and the gate voltage of M_{N11} increases until it turns on.
2) Then the startup current flows through M_{P2}, M_{P5}, and M_{N11} to GND.
3) As the startup current flows, the gate voltage of M_{N10} also increases, so that M_{N10} turns on. As a result, the electric charge in capacitor C_1 is charged with V_{DD}. Eventually, the gate voltage of M_{N11} drops to GND and it turns off; the operation as a startup circuit stops.

We see from Fig. 11 (V_{DD} rise time =1ms) that current I_X became 0 after the circuit started up. Therefore, the power consumption can be reduced compared to startup circuits 1 and 2.

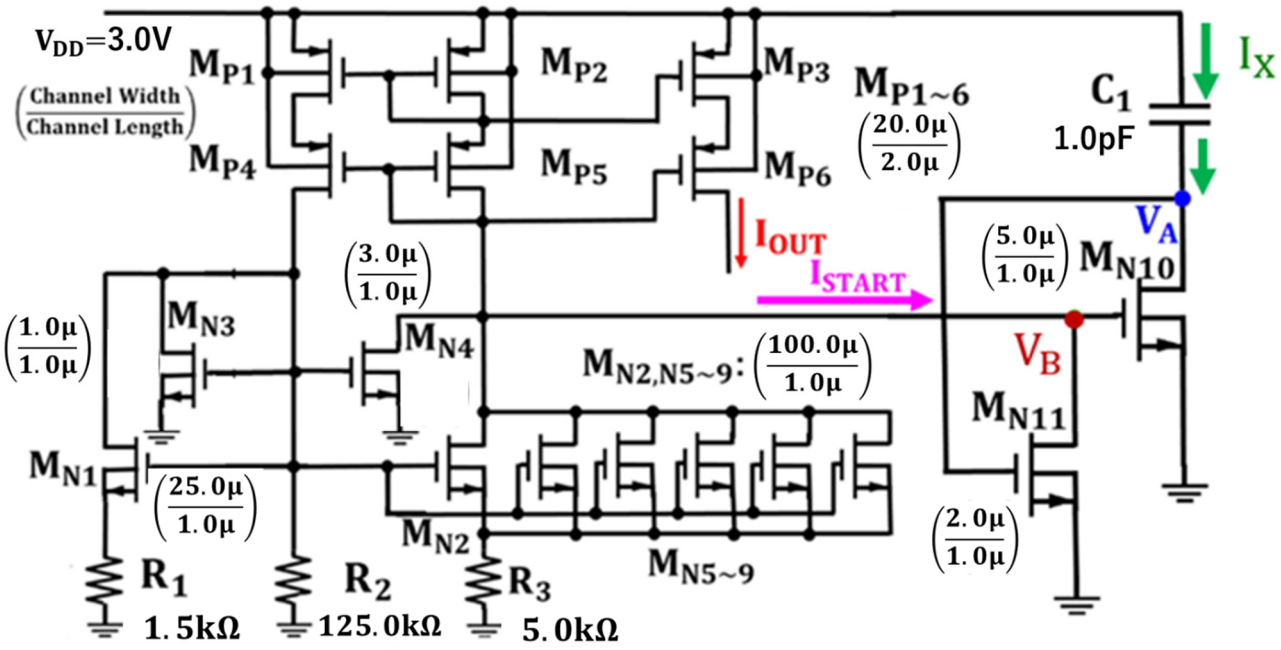

Fig. 10. GU reference current source with startup circuit 3.

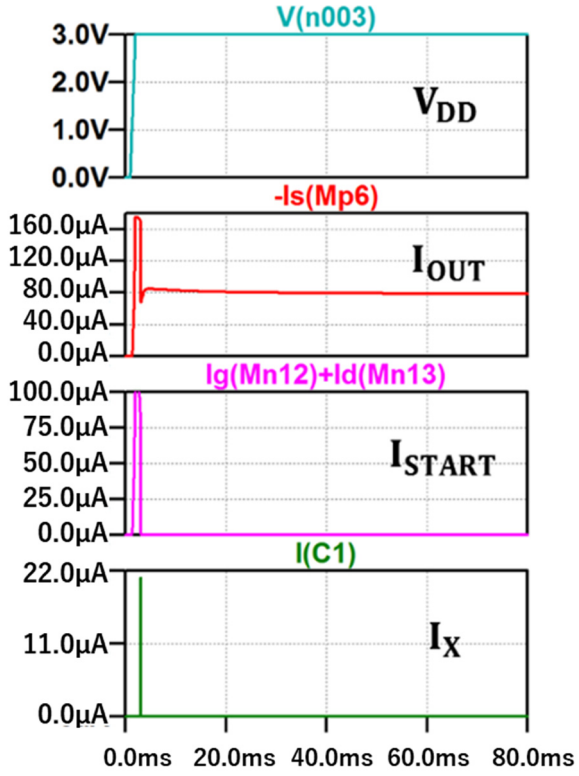

Fig. 11. Simulation result at 27°C (V_{DD} rise time =1ms).

However, startup circuit 3 has a potential risk in terms of startup operation reliability; when the power supply (V_{DD}) rises very slowly (i.e., $\Delta V_{DD}/\Delta t$ is very small), very small I_X suffices to charge C_1 so that V_A and V_B keep close to 0 and hence the proposed circuit does not start correctly. For example, as shown in Fig. 12, if the V_{DD} rise time is 81ms, startup fails and the desired I_{OUT} does not flow, whereas if the V_{DD} rise time is 1ms, it works properly. Furthermore, a large value of 1pF is chosen for the on-chip capacitor C_1, and the chip area is larger than that of startup circuits 1 and 2.

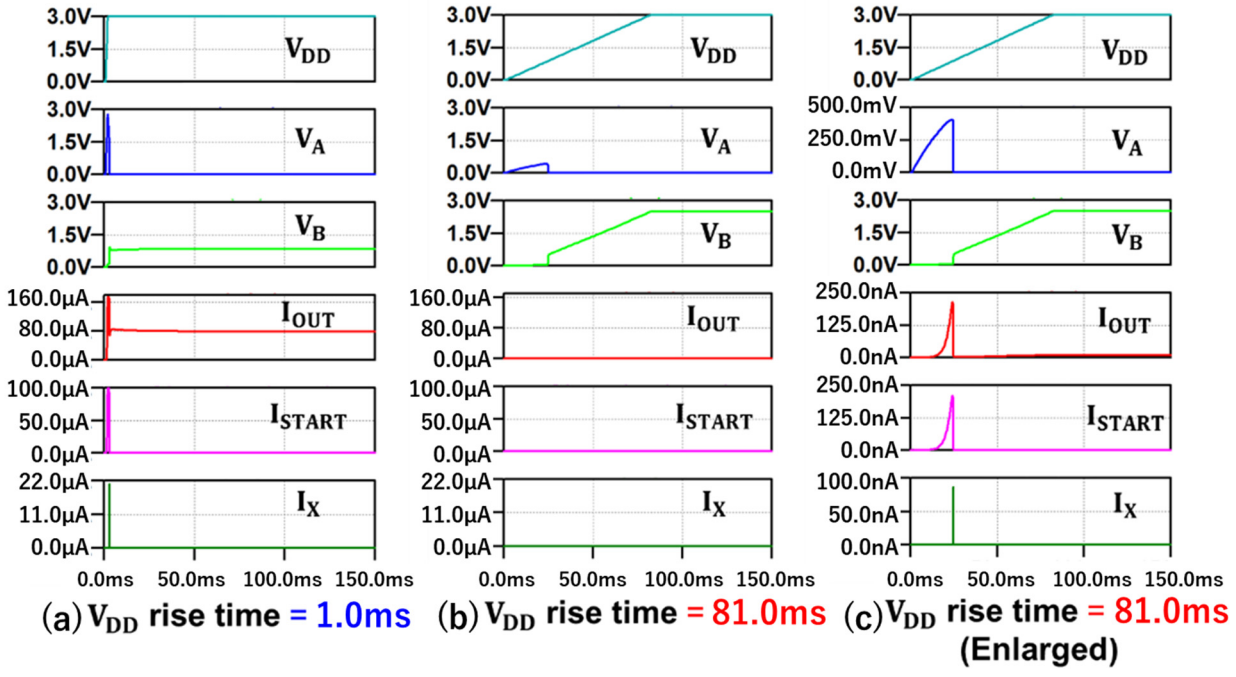

Fig. 12. Comparison between V_{DD} rise time of 1ms and 81 ms.

Fig. 13 shows the relationship between C_1 and the maximum V_{DD} rise time at which the startup operation of the circuit in Fig. 10 succeeds (limit value of V_{DD} rise time). Here an ideal capacitor model is assumed for C_1. The horizontal axis is the value of C_1 in Fig. 10, and the vertical axis is the limit value of V_{DD} rise time. As shown in Fig. 13, the larger C_1 is, the more the limit value of V_{DD} rise time can be increased.

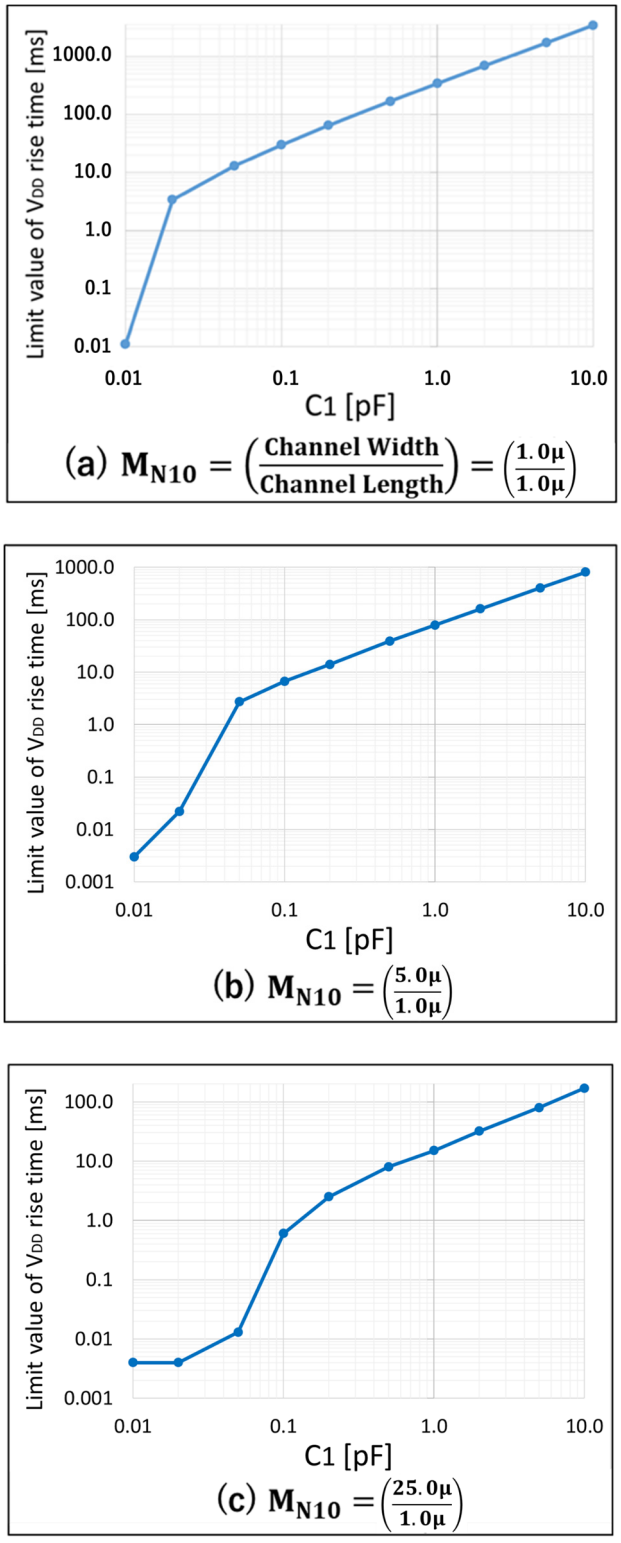

Fig. 13. Relationship between C_1 and the limit value of V_{DD} rise time.

Fig. 14 shows the relationship between M_{N10} channel width and the limit value of V_{DD} rise time when C_1 is 1pF in the circuit of Fig. 10. Here the M_{N10} channel length is 1μm. As shown in Fig. 14, the smaller the M_{N10} channel width is, the greater the limit value of V_{DD} rise time becomes.

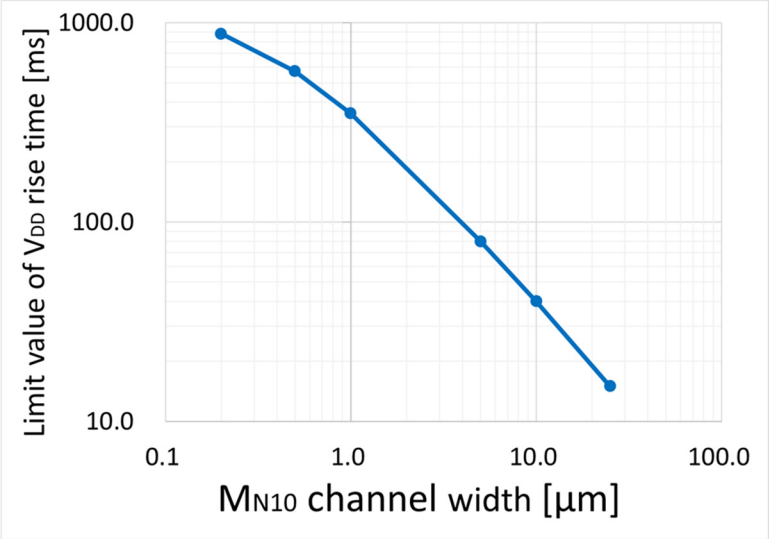

Fig. 14. Relationship between M_{N10} channel width and the limit value of V_{DD} rise time (C_1=1pF).

Fig. 15 shows the relationship between M_{N11} channel width and the limit value of V_{DD} rise time when C_1 is 1pF, and M_{N10} channel width is 5μm and channel length is 1μm in the circuit of Fig. 10. Here the M_{N11} channel length is 1 μm. As shown in Fig. 15, the larger M_{N11} channel width is, the greater the limit value of V_{DD} rise time can be.

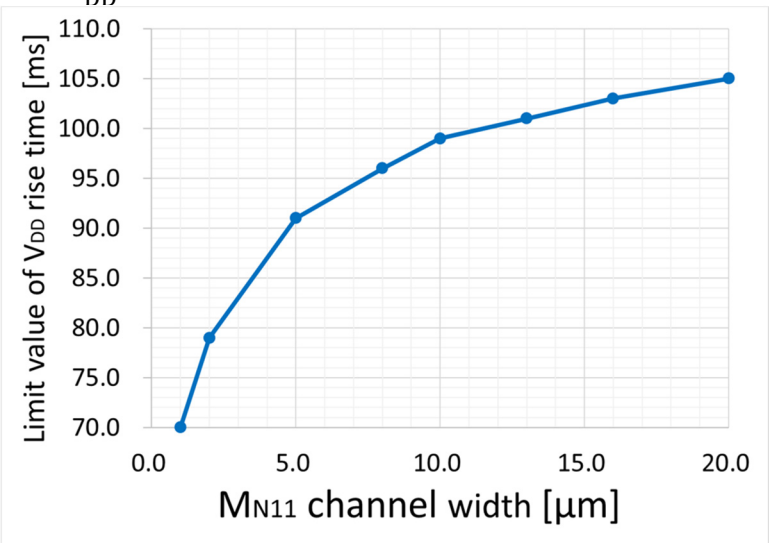

Fig. 15. Relationship between M_{N11} channel width and the limit value of V_{DD} rise time (C_1=1pF).

In summary, the limit value of V_{DD} rise time for correct startup operation increases as the value of capacitor C_1 is increased, (W/L) of M_{N10} is decreased and (W/L) of M_{N11} is increased. This can be interpreted as follows. Notice that

$$V_A(t) = V_{DD}(t) - Q(t)/C_1. \quad (2)$$

Where $Q(t)$ is the charge in C_1 at time t. At the startup time when $V_{DD}(t)$ rises, a finite amount of I_{START} has to flow to initiate stable startup operation so that $Q(t)/C_1$ should be very small and $V_A(t)$ follows $V_{DD}(t)$. In other words, large C_1 and small (W/L) of M_{N10} for small $I_x(t)$ are desirable for small $Q(t)/C_1$. Also, large (W/L) of M_{N11} is desirable for finite values of I_{START} given $V_A(t)$. Notice that for desirable operation, M_{N11} turns on after M_{P1} turns on.

Figs. 13, 14 and 15 show the design guideline for the values of C_1, (W/L) of M_{N10} and (W/L) of M_{N11} for a specified limit value of V_{DD} rise time. But notice that for example, in case of C_1=1pF in Fig. 13 (b), I_X= 3.0V/81ms × 1pF = 37pA; this is the order of the MOSFET leakage current. The operations of MOS transistors will change very much depending on temperature or process variations. So, Figs. 13, 14 and 15 are not so precise, but only show a tendency.

4.4 Comparison of Three Startup Circuits

The following table compares the three startup circuits.

Table. 1. Comparison of three types of startup circuits.

Type of startup circuits	Chip area	Power consumption	Startup reliability
Startup circuit 1	Good	Poor	Good
2 (CMOS inverter usage)	Fair	Fair	Good
3 (Capacitor usage)	Poor	Good	Poor

5. Conclusion

This paper introduced and simulated three types of startup circuits for our self-biasing MOS reference current source insensitive to supply temperature and voltage (Gunma University (GU) reference current source). We have compared them in terms of chip area, power consumption, and startup operation reliability. As a result, we found that each has its own advantages and disadvantages, and it is necessary to select the optimal startup circuit according to the application of the proposed circuit.

Comparison with similar CMOS reference current sources [17-20] is envisage as our next work.

Acknowledgements

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References

[1] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, ***John Wiley & Sons Inc.,*** 2009.

[2] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Fourth Edition, ***Wiley*****,** 2019.

[3] S. Yamamoto, K. I. Ebisawa, Y. Abe, T. Ida, Y. Shibasaki, N. Tsukiji, A. Kuwana, H. Kobayashi, A. Suzuki, Y. Todoroki, T. Kakinoki, N. Ono, K. Miura, "Operation and Stability Analysis of Temperature-Insensitive MOS Reference Current Source with Self-Bias Circuit", ***17th International SoC Design Conference*****,** (Yeosu, Korea) Oct. 2020.

[4] K. I. Ebisawa, S. Yamamoto, Y. Abe, T. Ida, Y. Shibasaki, A. Kuwana, H. Kobayashi, A. Suzuki, Y. Todoroki, T. Kakinoki, N. Ono, K. Miura, "Temperature-Insensitive MOS Reference Current

Source Circuit and its Startup Circuit", ***International Conference on Mechanical, Electrical and Medical Intelligent System,*** (Kiryu, Japan) Dec. 2019.

[5] L. Rolff, E. S. Bocholt, R. Wunderlich, S. Heinen, "An Integrated Low Drop Out Regulator with Independent Self Biasing Start Up Circuit", ***25th IEEE International Conference on Electronics, Circuits and Systems,*** (Bordeaux, France) Dec. 2018.

[6] A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff, B. H. Calhoun, "A 32nW Bandgap Reference Voltage Operational from 0.5V Supply for Ultra-Low Power Systems", ***IEEE International Solid-State Circuits Conference,*** (San Francisco, CA) Feb. 2015.

[7] N. Maghari, O. Shoaei, "A Dynamic Start-up Circuit for Low Voltage CMOS Current Mirrors with Power-Down Support", ***IEEE International Symposium on Circuits and Systems*****,** (Kobe, Japan) May. 2005.

[8] Z. Zhou, Y. Wang, Y. Shi, "A Bandgap Reference Using a Novel Soft Self-start Bias Circuit", ***IEEE Asia Pacific Conference on Circuits and Systems*****,** (Chengdu, China) Oct. 2018.

[9] Y.-T. Wang, C. Zhao, R. Geiger, D. Chen, S.-C. Huang, "Performance Verification of Start-up Circuits in Reference Generators", ***IEEE 55th International Midwest Symposium on Circuits and Systems,*** (Boise, ID) Aug. 2012.

[10] T. V. Cao, D. T. Wisland, T. S. Lande, F. Moradi, Y. H. Kim, "Novel Start-up Circuit with Enhanced Power-up Characteristic for Bandgap References", ***IEEE International SOC Conference,*** (Newport Beach) Sept. 2008.

[11] J. He, L. Zhao, Y. Cheng, "A 0.885ppm/°C Digitally Calibrated Bandgap Voltage Reference with Robust Start-up Circuit", ***12th IEEE International Conference on Solid-State and Integrated Circuit Technology,*** (Guilin, China) Oct. 2014.

[12] H. Shrimali, V. Liberali, "The Start-up Circuit for a Low Voltage Bandgap Reference", ***21st IEEE International Conference on Electronics, Circuits and Systems,*** (Marseille, France) Dec. 2014.

[13] C. Yu, L. Siek, "An Area-Efficient Current-Mode Bandgap Reference with Intrinsic Robust Start-Up Behavior", ***IEEE Transactions on Circuits and Systems II: Express Briefs,*** vol. 22, no. 10, pp. 937-941, Oct. 2015.

[14] K. Ueno, T. Hirose, T. Asai, Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs", ***IEEE Journal of Solid-State Circuits,*** vol. 44, no. 7, pp. 2047-2054, July. 2009.

[15] Y. Tsividis and C. McAndrew, Operation and Modeling of the MOS Transistor, 3rd Edition, ***Oxford University Press,*** Sept. 2012.

[16] S. Yamamoto, T. Hosono, T. Kamio, S. Katayama, K. I. Ebisawa, T. Feng, A. Kuwana, H. Kobayashi "Self-Biasing MOS Reference Current Sources Insensitive to Supply Voltage and Temperature", ***IEEE 3rd International Conference on Circuits and Systems,*** (Chengdu, China) Oct. 2021.

[17] T. Hosono, T. Kamio, S. Yamamoto, J. Matsuda, K. Hirai, S. Katayama, T. Feng, A. Kuwana, H. Kobayashi, A. Suzuki, S. Yamada, T. Kato, R. Kitakoga, T. Shimamura, G. Adhikari, N. Ono, K. Miura, "Nagata Current Sources with Self-Bias Configuration Insensitive to Supply Voltage and Temperature", ***IEEE International Conference on Electrical, Computer and Energy Technologies,*** (Cape Town, South Africa) Dec. 2021.

[18] T. Kamio, T. Hosono, S. Yamamoto, J. Matsuda, S. Katayama, A. Kuwana, A. Suzuki, S. Yamada, T. Kato, N. Ono, K. Miura, H. Kobayashi, "Design Consideration on MOS Peaking Current Sources Insensitive to Supply Voltage and Temperature", ***International Conference on Analog VLSI Circuits,*** (Bordeaux, France) Oct. 2021.

[19] T. Shima, "Temperature Insensitive Current Reference Circuit using Standard CMOS Devices", ***IEEE 50th Midwest Symposium on Circuits and Systems,*** (Montreal, Canada) Aug. 2007.

[20] Y.-T. Wang, D. Chen, R. L. Geiger, "A CMOS Supply-Insensitive with 13ppm/°C Temperature Coefficient Current Reference", ***IEEE 57th Midwest Symposium on Circuits and Systems,*** (College Station, TX) Aug. 2014.