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Self-Calibration of Two Reference Voltages Ratio for Two-Step Incremental Delta-Sigma ADC

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Abstract. This paper describes a two-step incremental ADC using the proposed self-calibration method. For high accuracy AD conversion, the ratio of the two reference voltages which are used in the two internal DACs should be accurately known. We propose here to measure their ratio using the incremental ADC itself, and it is stored in digital memory in self-calibration mode. Then in normal operation mode, the obtained two-step digital data are corrected in digital domain based on the measured and stored voltage ratio. This can be extended to a multi-step incremental ADC. The circuit configuration, self-calibration algorithm and behavioral simulation results are shown.

1. Introduction

Biosensors, Internet-of-Things and instrumentation applications require integrated sensor systems with high power efficiency, and ADCs are key elements in sensor interface circuits. In some applications, such as image sensors, a single ADC must be multiplexed among many channels, and an incremental ADC is suitable there due to its circuit simplicity, low power and high accuracy. In recently years, there are plenty of research activities in this area [1-9]. The one-step incremental ADC takes a long time AD conversion time and hence the two-step incremental ADC is proposed which can speed-up the AD conversion. However, the mismatch between step 1 and step 2 operation circuits causes the overall ADC nonlinearity.

In this paper, we propose a self-calibration method for the two-step incremental ADC, where the reference voltage V_{r2} for the step 2 operation is measured using the step 1 operation circuit and reference voltage V_{r1}, and the measured data is stored in digital memory in calibration mode. Then based on the stored data, the output data is corrected in digital domain in normal operation mode. Its circuit configuration, operation and simulation results are shown.

This paper is organized as follows: Section 2 explains the one-step incremental ADC, and Section 3 shows the two-step incremental ADC and its simulation results. Section 4 describes the proposed self-calibration and simulation verification. Section 5 provides conclusion.

2. One-step incremental ADC

Fig. 1 shows the first-order one-step incremental ADC with the input range of Vin between -Vr1 to Vr1. Fig. 1 (a) shows its circuit configuration and Fig. 1 (b) shows its timing chart. Its configuration resembles to the ΔΣ ADC. However, when its operation starts, the integrator and the counter are reset, and it is a Nyquist-rate ADC instead of an oversampling ADC. In some aspects, it is similar to the integrating ADC [10]. The one-step incremental ADC takes 2^n clock cycles to realize n-bit resolution AD conversion. For example, in $n = 16$ case, 65,536 cycles are required, which takes a long conversion time. Then the two-step incremental ADC is considered to alleviate this problem, as described in the next section.

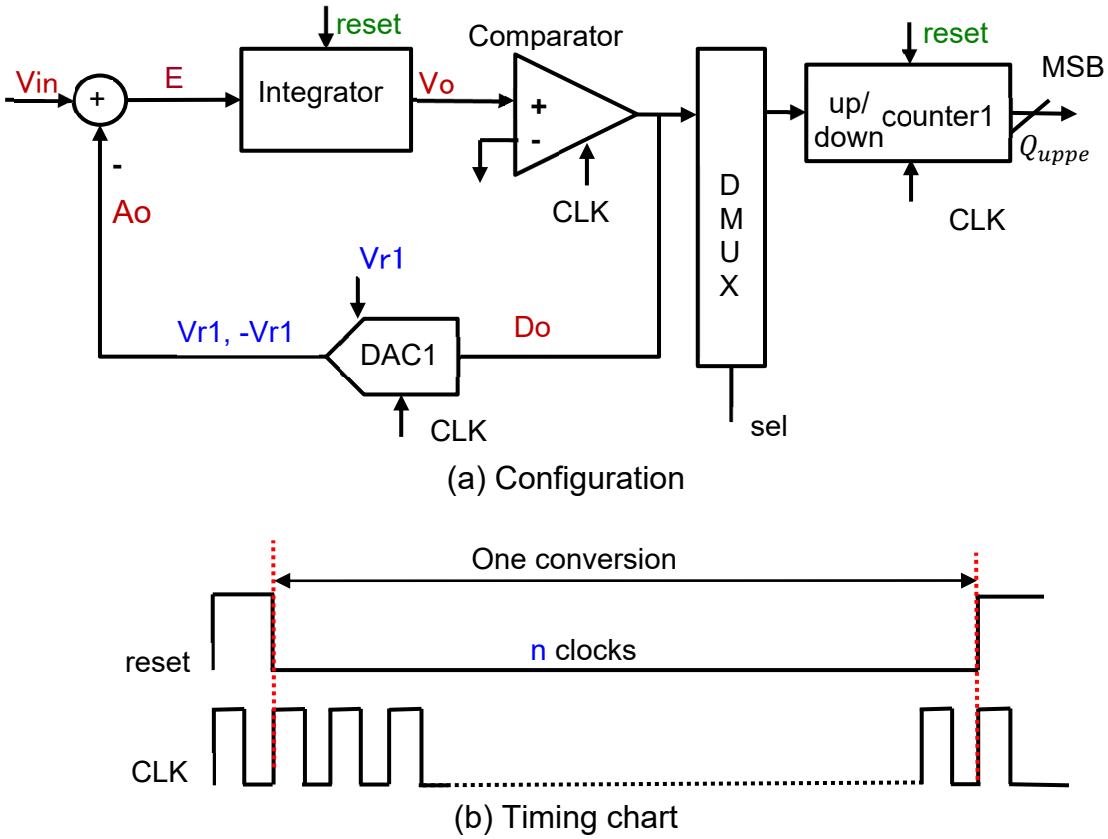


Fig.1. One-step first-order incremental ADC.

3. Two-step incremental ADC

Fig. 2 shows the first-order two-step incremental ADC. Fig. 2 (a) shows its configuration, while Fig. 3 shows its timing chart. It is composed of an analog integrator with reset, a comparator, two 1-bit DACs (DAC1, DAC2) and two counters with reset. DAC1 outputs V_{r1} for the digital input D_0 of 1 and $-V_{r1}$ for 0, whereas DAC2 outputs V_{r2} for 1 and $-V_{r2}$ for 0. These outputs are selected by a select signal (sel) and a multiplexer (MUX), and then it is fed-back to the analog integrator. The comparator output D_0 is provided to one of 2 counters with reset, which is selected with the select signal (sel) and a de-multiplexer (DMUX).

3.1 Step 1 Operation

In the operation at the step 1 (Fig. 2 (b)), the analog integrator and 2 counters are reset to zero. Then the DC input V_{in} is provided. DAC1 is selected and the difference between V_{in} and the DAC1 output A_{01} is input to the analog integrator and accumulated.

When the analog integrator V_0 is positive or zero, then the comparator produces the output D_0 of 1 at the rising edge of the clock (CLK). The counter1 output is incremented by 1, and the DAC1 output A_{01} is V_{r1}. When V_0 is negative, then the comparator output D_0 is 0. The counter output1 is decremented by 1, and A_{01} is $-V_{r1}$. These operations are repeated by N clock cycles, and the counter1 output is obtained as Q_{upper}.

This operation algorithm at step 1 can be written as follows:

For $n = 1$ to N:

$$V_0(1) = 0, Q_{upper}(1) = 0, D_0(1) = 0, A_0(1) = V_{r1}.$$
$$E(n) = V_{in}(n) - A_0(n)$$
$$V_0(n+1) = V_0(n) + E(n)$$

If $(V_0(n+1) \geq 0)$, then

$D_0(n+1) = 1$

$Q_{upper}(n+1) = Q_{upper}(n) + 1$

$A_0(n+1) = V_{r1}$

Else if$(V_0(n+1) < 0)$, then

$D_0(n+1) = 0$

$Q_{upper}(n+1) = Q_{upper}(n) - 1$

$A_0(n+1) = -V_{r1}.$

After N cycles, $Q_{upper}(N+1)$ shows the following:

N_p: the number of the comparator output $D_0 = 1$.

N_m: the number of the comparator output $D_0 = 0$.

Here $Q_{upper}(N+1) = N_p - N_m, \quad N = N_p + N_m$.

Then $V_0(N+1) = N \cdot V_{in} - (N_p - N_m)V_{r1}$.

3.2 Step 2 Operation

In the operation at the step two (Fig. 2 (c)), the input V_{in} is set to zero. At its operation start time, the analog integrator output value is kept as the final value at the step 1 and counter2 starts from zero. DAC2 is selected and the difference between V_{in} and the DAC2 output A_{02} is input to the analog integrator and accumulated.

Similarly, when the analog integrator V_0 is positive or zero, then the comparator produces the output D_0 of 1 at the rising edge of the clock (CLK). The counter2 output is incremented by 1, and the DAC2 output A_{02} is V_{r2}. When V_0 is negative, then the comparator output D_0 is 0. The counter output2 is decremented by 1, and A_{o2} is $-V_{r2}$. These operations are repeated by M clock cycles, and the counter2 output is obtained as Q_{lower}.

This operation algorithm at step 2 can be written as follows:

$$Q_{lower}(N+1) = 0$$

For $n = N+1$ to $N+M$:

$$E(n+1) = -A_0(n+1)$$
$$V_0(n+1) = V_0(n) + E(n)$$

If$(V_0(n+1) \geq 0)$
$D_0(n+1) = 1$
$Q_{lower}(n+1) = Q_{lower}(n) + 1$
$A_0(n+1) = V_{r2}$

Else if$(V_0(n+1) < 0)$
$D_0(n+1) = 0$
$Q_{lower}(n+1) = Q_{lower}(n) - 1$
$A_0(n+1) = -V_{r2}$

After $N+M$ cycles, $Q_{lower}(N+M+1)$ shows the following:
M_p: the number of the comparator output $D_0 = 1$.
M_m: the number of the comparator output $D_0 = 0$.
Here $Q_{lower}(N+M+1) = M_p - M_m$, $M = M_p + M_m - 1$.
Then we have the following:

$$V_0(N+M+1) = N \cdot V_{in} - (N_p - N_m)V_{r1} - (M_p - M_m)V_{r2}$$

$$N \cdot V_{in} - (N_p - N_m)V_{r1} - (M_p - M_m)V_{r2} \fallingdotseq 0$$

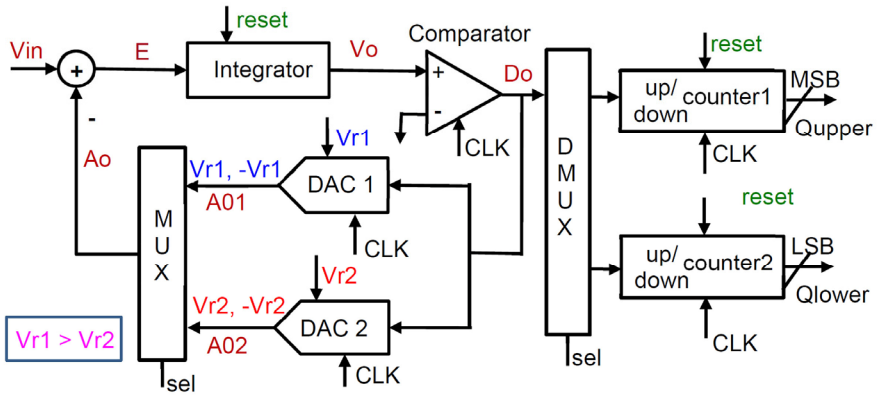
$$V_{in} = \frac{N_p - N_m}{N} V_{r1} + \frac{M_p - M_m - 1}{N} V_{r2}$$

$$V_{in} = V_{r1}\left\{\left[2 \cdot \frac{N_p}{N} - 1\right] + K \cdot \left[2 \cdot \frac{M_p}{M-1} - 1\right]\frac{M-1}{N}\right\} \quad (1)$$

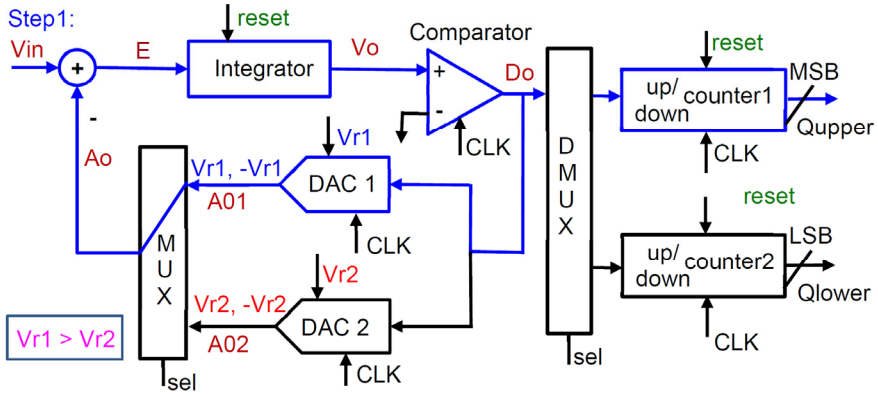
The analog input V_{in} can be measured as the following:

Digital output $\left[2 \cdot \frac{N_p}{N} - 1\right] + K \cdot \left[2 \cdot \frac{M_p}{M-1} - 1\right]\frac{M-1}{N}$

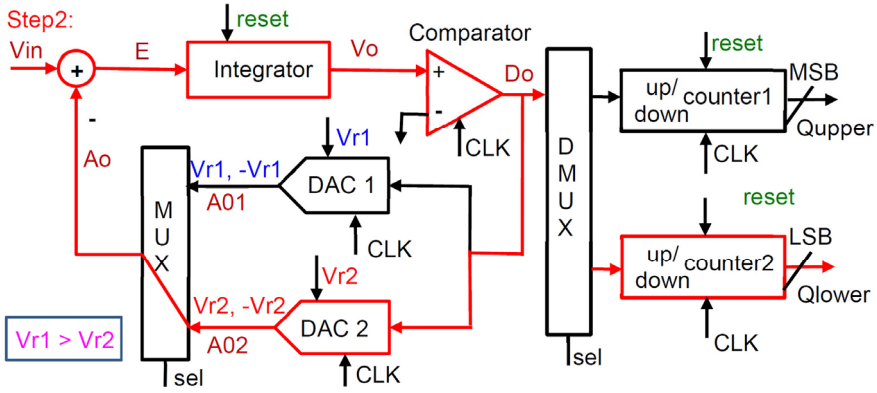
Here $K = V_{r2}/V_{r1}$, and we need to know its exact value.



(a) Configuration



(b) Operation step 1



(c) Operation step2

Fig. 2. Two-step incremental ADC.

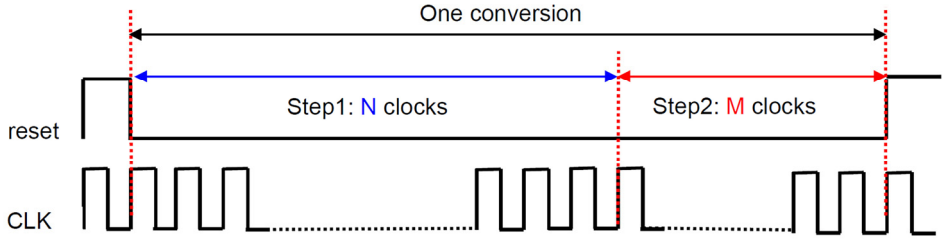


Fig. 3. Two-step incremental ADC operation timing chart.

3.3 Two-step incremental ADC simulation verification

The simulation result of two-step incremental ADC with only operation step 1 shown in Fig. 4. The result shows that when the clock numbers increase the error between the input V_{in} simulation and V_{in} calculation (evaluated by Eq. (1)) is reduced.

Here, y-axis in Fig. 3 denotes the normalized absolute error between the exact input voltage which symbolized as V_{in} simulation and the input voltage evaluated by Eq. (1) which is symbolized as V_{in} calculation:

$$\text{Normalized absolute error} = max_{Vin} \ |V_{in} \text{ simulation} - V_{in} \text{ calculation}| \quad (2)$$

For $1/2^n$ accuracy, 2^n clocks are required and for high accuracy, it takes long conversion time.

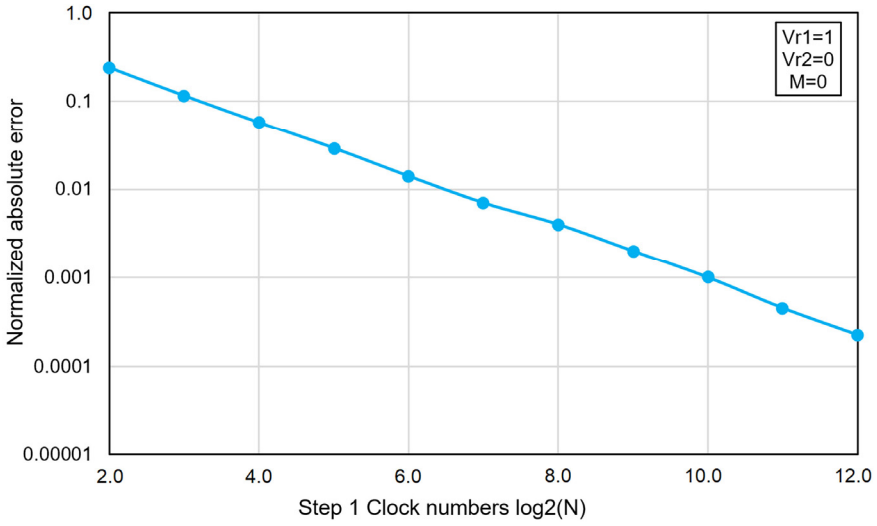


Fig. 4. Simulation results of two-step incremental ADC with only operation step 1.

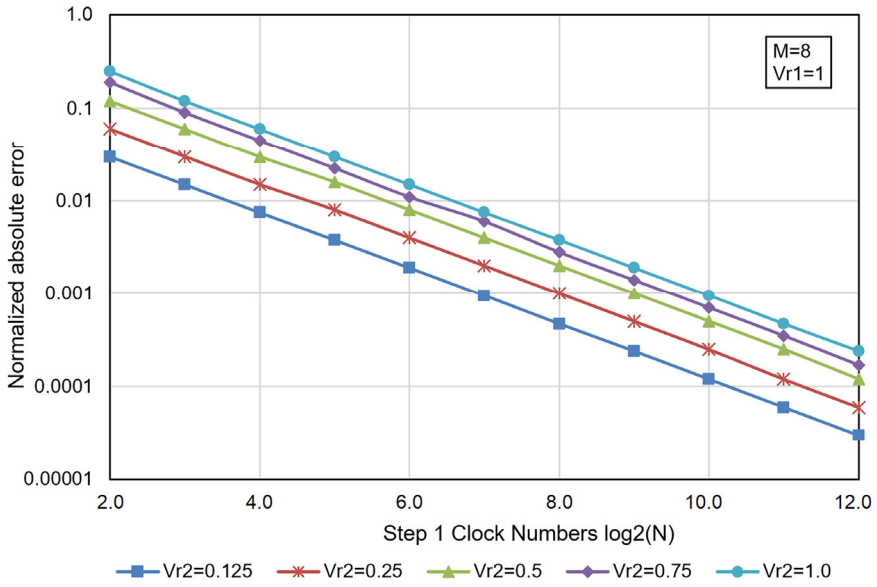
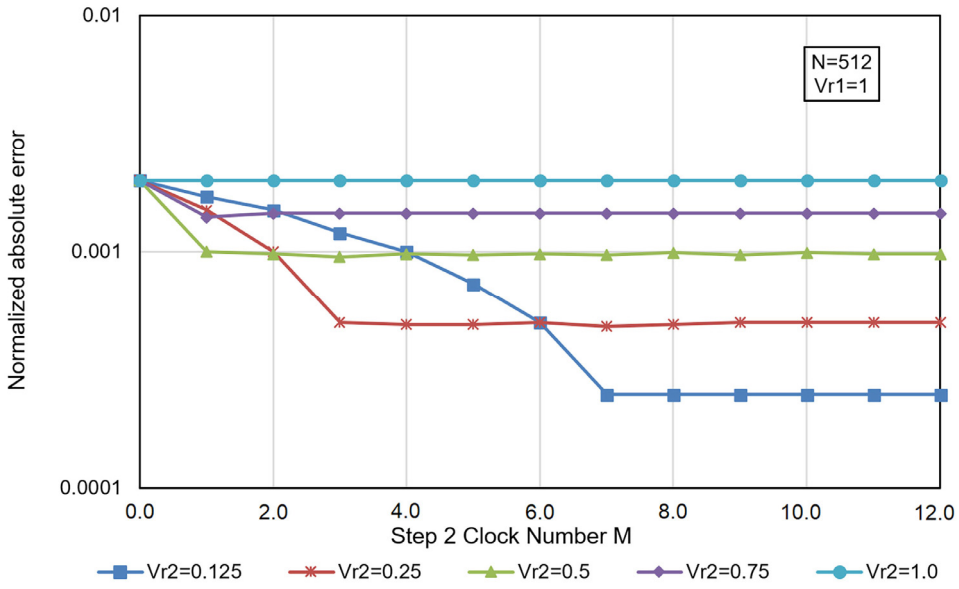
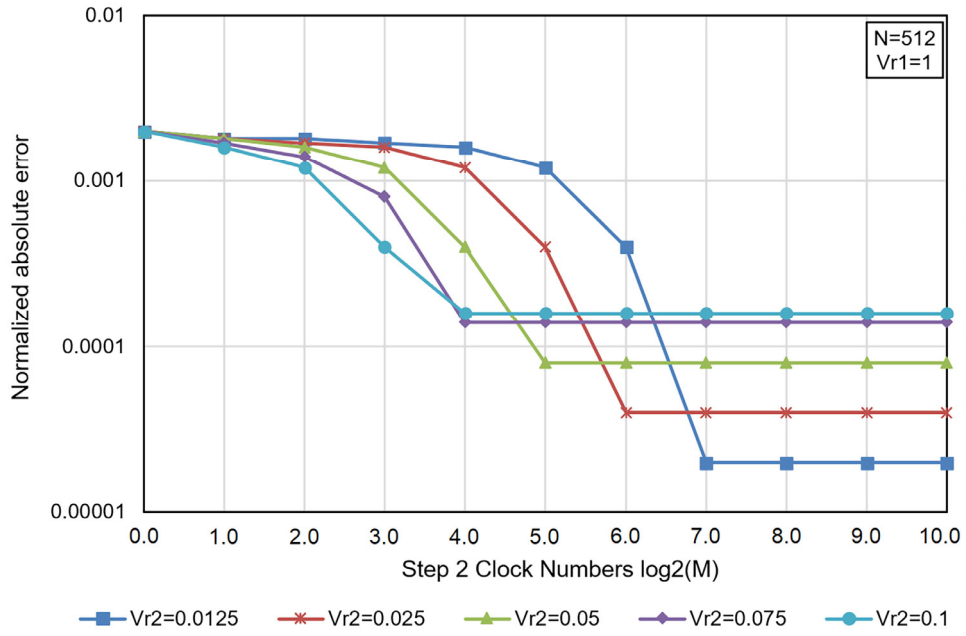


Fig. 5. Simulation results of the two-step incremental ADC as a parameter of the reference voltage Vr2 with the various number N of the step 1 clock cycles and the fixed number M (=8) of the step 2 clock cycles.



(a) The number of step 1 clock cycles N=512



(b) With the reference voltage Vr2, which is 10 times smaller than that in Fig. 5 (a)

Fig. 6. Simulation results of the two-step incremental ADC as a parameter of the reference voltage Vr2 with the various number M of the step 2 clock cycles.

The simulation results of the two-step incremental ADC with the operations of step 1 and step 2 are shown in Fig. 5. First, we consider the number N of the operation step 1 clock cycles with increase by 2 times. We found that the error of the incremental ADC decreases to half for 2 times increase of N. Then we consider the effect of the reference voltage V_{r2} of the operation step 2 in four cases: $V_{r2} = 0.125, 0.25, 0.5, 0.75, 1$. We found that in the case of the reference voltage $V_{r2} < V_{r1}$, the AD conversion error is decreased as the reference voltage V_{r2} is decreased. In the case of $V_{r2} = V_{r1}$, the error is equal to operation step 1 only as shown in Fig.4.

Fig. 6 shows the simulation results by considering the number of the operation step 2 clock cycles M in four cases of the reference voltage V_{r2}. First, we set $N = 512$ as a fixed value and increase M from 0 to 12 in four cases of the reference voltage V_{r2}. Here, $M = 0$ means that only operation step 1 is performed. The simulation result is shown in Fig. 6 (a), and we see that the smallest $V_{r2}(= 0.125)$ provides a substantial decrease of error while it needs a large number M of clock cycles in operation step 2. Then, we considered the smaller V_{r2} case that $V_{r2} = 0.0125, 0.025, 0.050, 0.075, 0.1$, and the simulation result is shown in Fig. 6 (b). We found that small V_{r2} could reduce the error significantly, but more clock cycles in operation step 2 are needed.

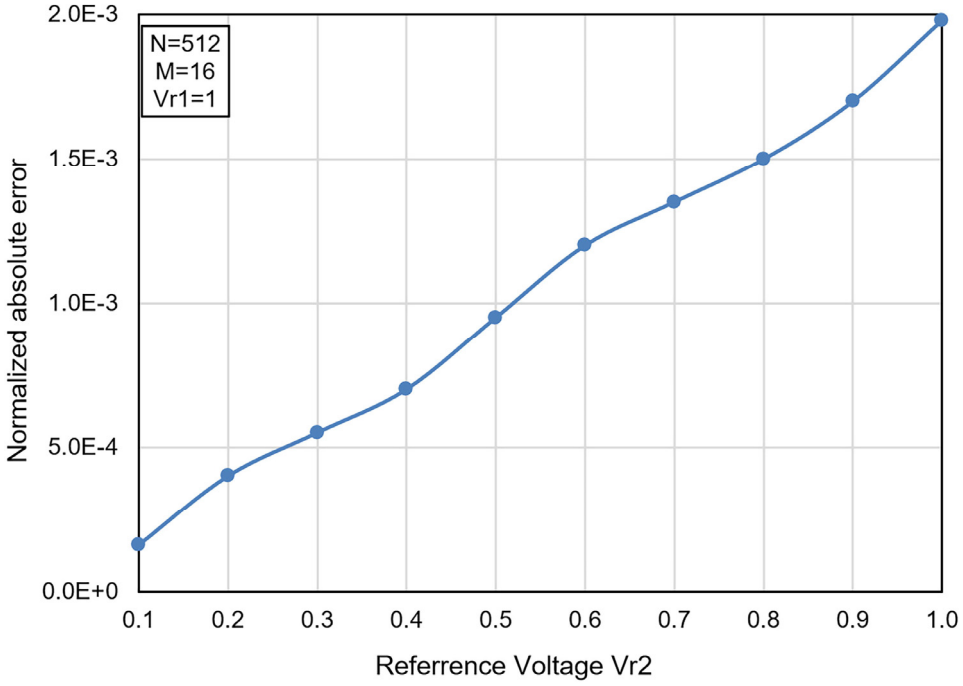


Fig. 7. Simulation results of the two-step incremental ADC operation step 2 with various reference voltage Vr2 for N=512 and M=16.

Fig. 7 shows the simulation result of the two-step incremental ADC in operation step 2 to clarify the effect of the reference voltage V_{r2}. The result shows the error between V_{in} and ADC output is proportional to the reference voltage V_{r2}. According to the simulation results above, for the error less than $1/2^{16}$, it is necessary that $N = 1024, M = 128$ where the reference voltage $V_{r2} = 0.0125, V_{r1} = 1$.

4. Self-Calibration for two reference voltages

In an actual chip, there can be some mismatch between DAC1 and DAC2, or their gain ratio is not as expected, then the overall ADC accuracy degrades. We consider here that DAC1 uses the reference voltage V_{r1} while DAC2 uses V_{r2}. Their exact ratio cannot be implemented as designed due to process variation, so that it has to be measured accurately.

We propose here that in self-calibration mode, V_{r2} is measured with the incremental ADC using the reference voltage V_{r1}. Then the ratio V_{r2}/V_{r1} can be obtained with high accuracy.

$$V_0(1) = 0, Q_{upper}(1) = 0, D_0(1) = 0, A_0(1) = V_{r1}$$
$$E(n) = V_{r2} - A_0(n)$$
$$V_0(n+1) = V_0(n) + E(n)$$

If $(V_0(n+1) \geq 0)$
$D_0(n+1) = 1$
$Q_{upper}(n+1) = Q_{upper}(n) + 1$
$A_0(n+1) = V_{r1}$
Else if$(V_0(n+1) < 0)$
$D_0(n+1) = 0$
$Q_{upper}(n+1) = Q_{upper}(n) - 1$
$A_0(n+1) = -V_{r1}$
After L cycles,
L_p: the number of the digital output for $D_0 = 1$.
L_m: the number of the digital output for $D_0 = 0$.
Here $L = L_p + L_m$.
Then $V_0(L+1) = L \cdot V_{r2} - (L_p - L_m)V_{r1}$.
Since $V_0(L+1) \fallingdotseq 0$, we have the following:

$$K = V_{r2}/V_{r1} \fallingdotseq (L_p - L_m)/L \quad (3)$$

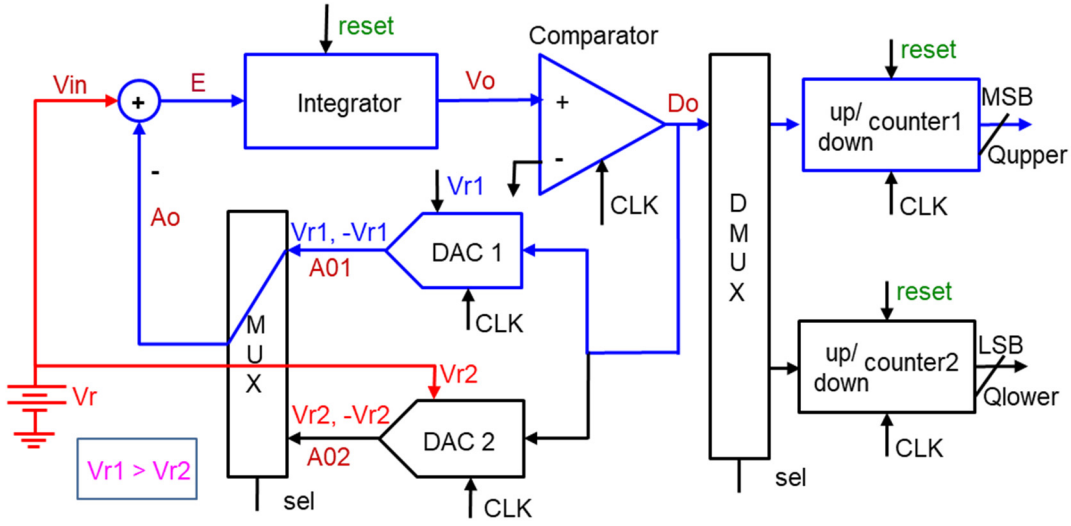
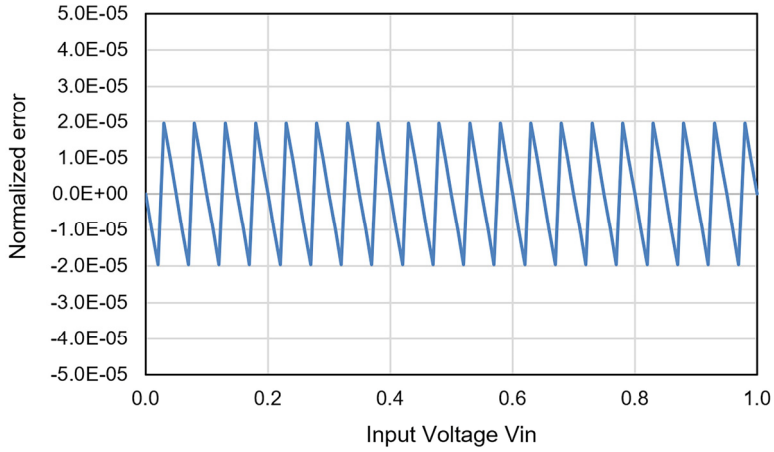


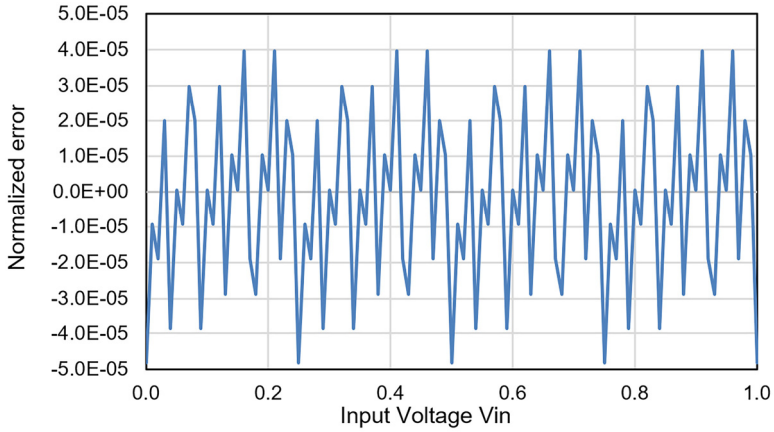
Fig. 8. Self-calibration mode: Vr2 is measured using the incremental ADC circuit itself with the reference voltage Vr1.

Fig. 9 shows the simulation verification of the proposed self-calibration. Fig. 9 (a) shows the simulation result in ideal case: $V_{r1} = 1, V_{r2} = 0.0125$ and $K = 0.0125$. Here K is the coefficient in Eq. (2). Notice that y-axis in Fig. 9 denotes the normalized error between the exact input voltage which symbolized as V_{in} simulation and input voltage evaluated by Eq. (1) which is symbolized as V_{in} calculation:

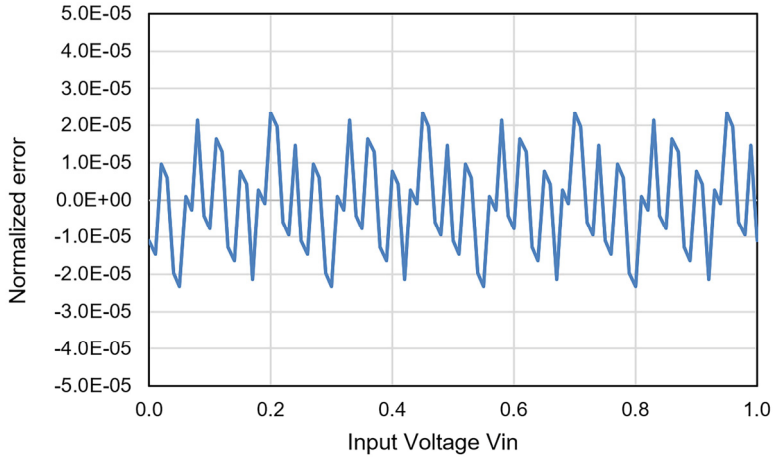
$$\text{Normalized error} = (V_{in}\, simulation - V_{in}\, calculation) \quad (4)$$



(a) Ideal case.



(b) Without calibration



(c) With calibration

Fig. 9. Simulation results of self-calibration for N=512, M=128.

Fig. 9 (b) and (c) show the case that there is a deviation of the actual $V_{r2} = 0.01275$ from the designed value of $V_{r2} = 0.0125$, while $V_{r1} = 1$. In other words, the actual ratio of $V_{r2}/V_{r1} = 0.01275$. Fig. 9 (b) shows the simulation results without self-calibration, where we use $K = 0.0125$ for the calculation. We see larger error compared to those in Fig. 9 (a).

Fig. 9 (c) shows the simulation result with self-calibration. The measurement in self-calibration shows that $V_{r2} = 0.012748$. Fig. 9 (c) is obtained using $V_{r1} = 1, V_{r2} = 0.0125$, and $K = 0.012748$, which shows that the errors become smaller compared to those in Fig. 9 (b) and comparable to those in Fig. 9 (a).

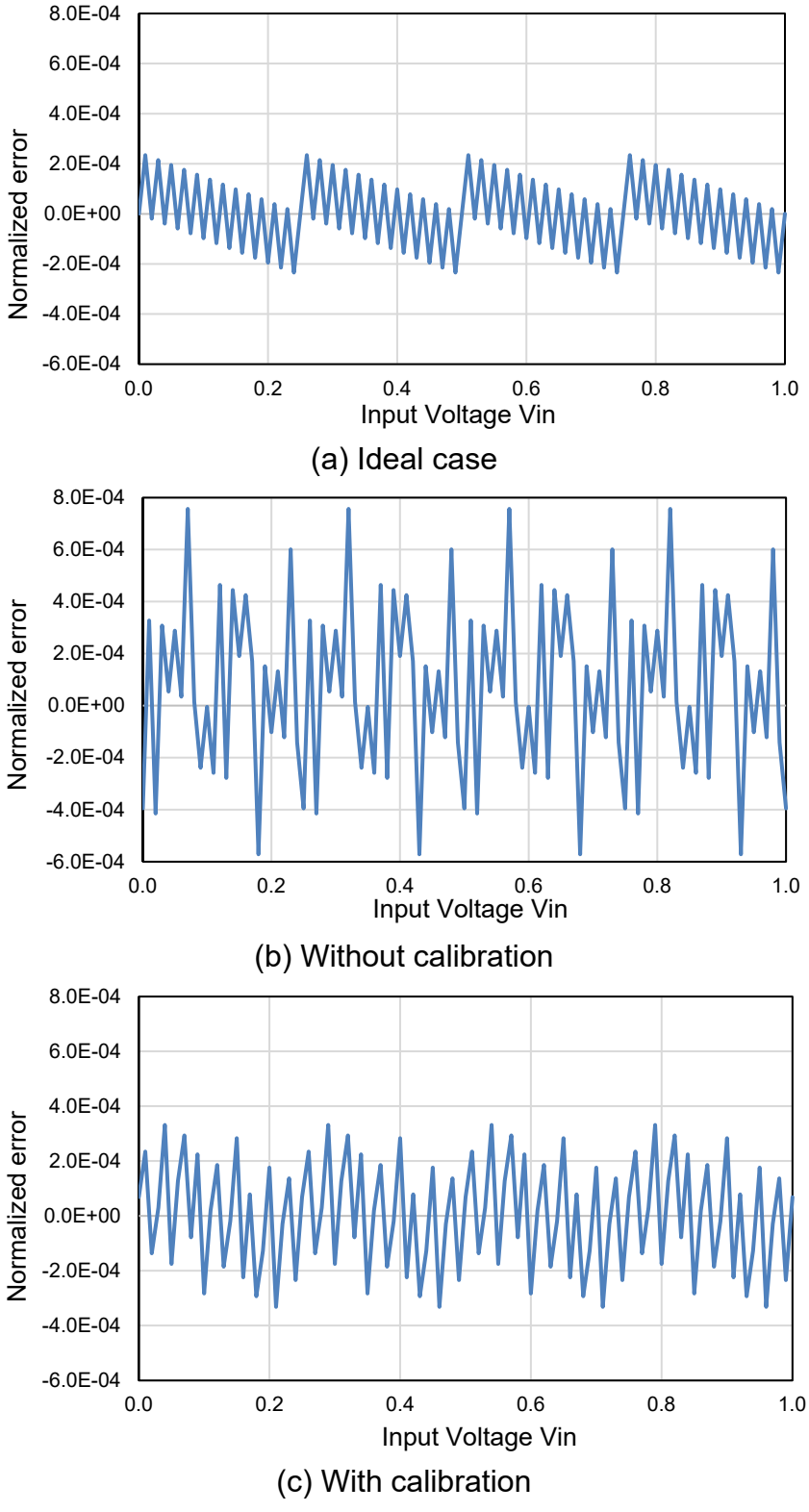


Fig. 10 Simulation results of self-calibration for N=512, M=16.

The simulation results in Fig. 10 are similar to those in Fig. 10, where a larger value of reference voltage $V_{r2} = 0.125$ is used. Fig. 10 (a) shows the ideal case. Fig. 10 (b) shows the mismatch case without calibration, where $V_{r1} = 1, V_{r2} = 0.1725$ and $K = 0.125$. Fig. 10 (c) shows that with self-calibration, where $V_{r1} = 1, V_{r2} = 0.1725$ and $K = 0.17248$. Here, the value of $K = 0.17248$ is measured in self-calibration mode. We see that the errors in Fig. 10 (c) become smaller than those in Fig. 10 (b).

Remarks:

(i) For high accuracy measurement of $K = V_{r2}/V_{r1}$, the number of cycles is large, but notice that this is just one time. Then the value of K is stored in memory and it is used for normal operation to correct the digital output.

(ii) The calculation of K multiplied by Q_{upper} can be done with an adder and a barrel-shifter; in other words, an expensive floating-point multiplier is not necessary. Suppose that $Q_{upper} = b_n b_{n-1} b_{n-2} \ldots b_0$ in binary format, where $b_n = 1$ or 0 $(k = n, n-1, \ldots, 1, 0)$. Then $K \times Q_{lower}$ is calculated as follows:

$$K \times Q_{upper} = \sum_{m \text{ for } b_m=1} K \times 2^m \tag{5}$$

$K \times 2^m$ can be obtained with m-bit left shift of K.

(iii) One may ponder that since Vr1 > Vr2, it seems more accurate to measure Vr1 with Vr2 in calibration. However, you cannot do such a way because the incremental AD modulator will saturate and not work correctly for Vin = Vr1, Vref =Vr2 and 0< Vr2 < Vr1. Vin must be between –Vref and Vref.

Notice that Table 1. summarizes the simulation key-parameters.

Table 1. Simulation key-parameters for each simulation.

		Vin	Vr1	Vr2	K	N	M
Fig.3		0.1-1	1	N/A		$2\sim2^{12}$	0
Fig.4		0.1~1	1	0.125 0.25 0.50 1.0		$2\sim2^{12}$	8
Fig.5	(a)	0.1~1	1	0.125 0.25 0.50 1.0		512	0~10
	(b)	0.1~1	1	0.0125 0.025 0.050 0.100		512	$0\sim2^{10}$
Fig.6		0.1~1	1	0.1~1		512	16
Fig.8	(a)	0.1~1	1	0.0125	0.01250	512	128
	(b)		1	0.0125	0.01275		
	(c)		1	0.0125	0.01248		
Fig.9	(a)	0.1~1	1	0.125	0.1250	512	16
	(b)		1	0.1725	0.1250		
	(c)		1	0.1725	0.17248		

5. Conclusion

In this paper, we have proposed a self-calibration method for the two-step incremental ADC. First, the two-step incremental ADC configuration and its behavior are verified by simulations Then the proposed self-calibration method to compensate for the mismatches between the first step and second step operation circuits is shown with behavioral simulation verification.

We will extend this method to three-step and four-step incremental ADCs.

Acknowledgements

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